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HD404318 Series

Rev. 6.0
Sept. 1998

Description

The HD404318 Series is 4-bit HMCS400-series microcomputer with large-capacity memory designed to increase program productivity. Each microcomputer has an A/D converter and input capture timer built in. They also come with high-voltage I/O pins that can directly drive a fluorescent display.

The HD404318 Series includes four chips: the HD404318 with 8-kword ROM; the HD404316 with 6-kword ROM; the HD404314 with 4-kword ROM; the HD4074318 with 8-kword PROM.

The HD4074318 is a PROM version ZTAT™ microcomputer. Programs can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi Ltd.

Features

- 34 I/O pins
  - One input-only pin
  - 33 input/output pins: 21 pins are high-voltage pins (40 V, max.)
- On-chip A/D converter (8-bit × 8-channel)
- Three timers
  - One event counter input
  - One timer output
  - One input capture timer
- 8-bit clock-synchronous serial interface (1 channel)
- Alarm output
- Built-in oscillators
  - Ceramic or crystal oscillator
  - External clock drive is also possible

- Seven interrupt sources
  - — Two by external sources
  - — Three by timers
  - — One each by the A/D converter and serial interface
- Two low-power dissipation modes
  - — Standby mode
  - — Stop mode
- Instruction cycle time 1 µs (f_{osc} = 4 MHz)

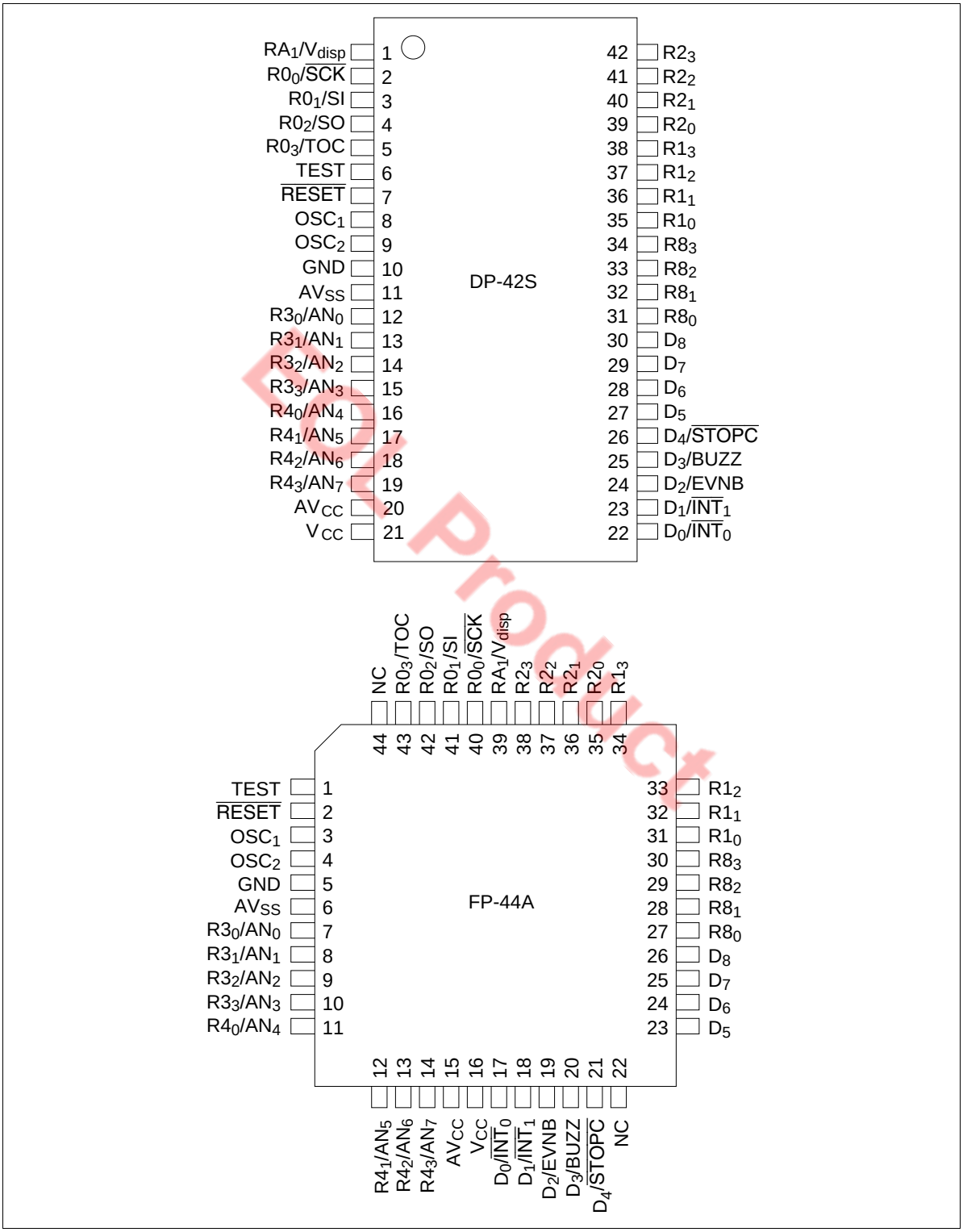
Ordering Information

Type	Model Name	ROM (words)	RAM (digit)	Package
Mask ROM	HD404314S	4,096	384	DP-42S
	HD404314H			FP-44A
	HD404316S	6,144		DP-42S
	HD404316H			FP-44A
	HD404318S	8,192		DP-42S
	HD404318H			FP-44A
ZTAT™	HD4074318S	8,192		DP-42S
	HD4074318H			FP-44A

Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacture	**Model Name**	**Package**	**Manufacturer**	**Model Name**
DATA I/O Corp.	121B	DP-42S	Hitachi	HS4318ESS01H
		FP-44A		HS4318ESH01H
AVAL Corp.	PKW-1000	DP-42S	Hitachi	HS4318ESS01H
		FP-44A		HS4318ESH01H

Pin Arrangement



PinDescription

Item	Symbol	Pin Number DP-42S	Pin Number FP-44A	I/O	Function
Power supply	V_{CC}	21	16		Applies power voltage
	GND	10	5		Connected to ground
	V_{disp} (shared with RA_1)	1	39		Used as a high-voltage output power supply pin when selected by the mask option
Test	TEST	6	1	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	7	2	I	Resets the MCU
Oscillator	OSC_1	8	3	I	Input/output pin for the internal oscillator. Connect these pins to the ceramic or crystal oscillator, or OSC_1 to an external oscillator circuit.
	OSC_2	9	4	O	
Port	D_0–D_8	22–30	17–21, 23–26	I/O	Input/output pins addressed individually by bits; D_0–D_8 are all high-voltage I/O pins. Each pin can be individually configured as selected by the mask option.
	RA_1	1	39	I	One-bit high-voltage input port pin
	$R0_0$–$R0_3$, $R3_0$–$R4_3$	2–5, 12–19	40–43, 7–14	I/O	Four-bit input/output pins consisting of standard voltage pins
	$R1_0$–$R2_3$, $R8_0$–$R8_3$	31–42	27–38	I/O	Four-bit input/output pins consisting of high voltage pins
Interrupt	$\overline{INT_0}$, $\overline{INT_1}$	22, 23	17, 18	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	26	21	I	Input pin for transition from stop mode to active mode
Serial interface	$\overline{SCK}$	2	40	I/O	Serial interface clock input/output pin
	SI	3	41	I	Serial interface receive data input pin
	SO	4	42	O	Serial interface transmit data output pin
Timer	TOC	5	43	O	Timer output pin
	EVNB	24	19	I	Event count input pin
Alarm	BUZZ	25	20	O	Square waveform output pin
A/D converter	AV_{CC}	20	15		Power supply for the A/D converter. Connect this pin as close as possible to the V_{CC} pin and at the same voltage as V_{CC}. If the power supply voltage to be used for the A/D converter is not equal to V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
	AV_{SS}	11	6		Ground for the A/D converter. Connect this pin as close as possible to GND at the same voltage as GND.
	AN_0–AN_7	12–19	7–14	I	Analog input pins for the A/D converter

Pin Description in PROM Mode

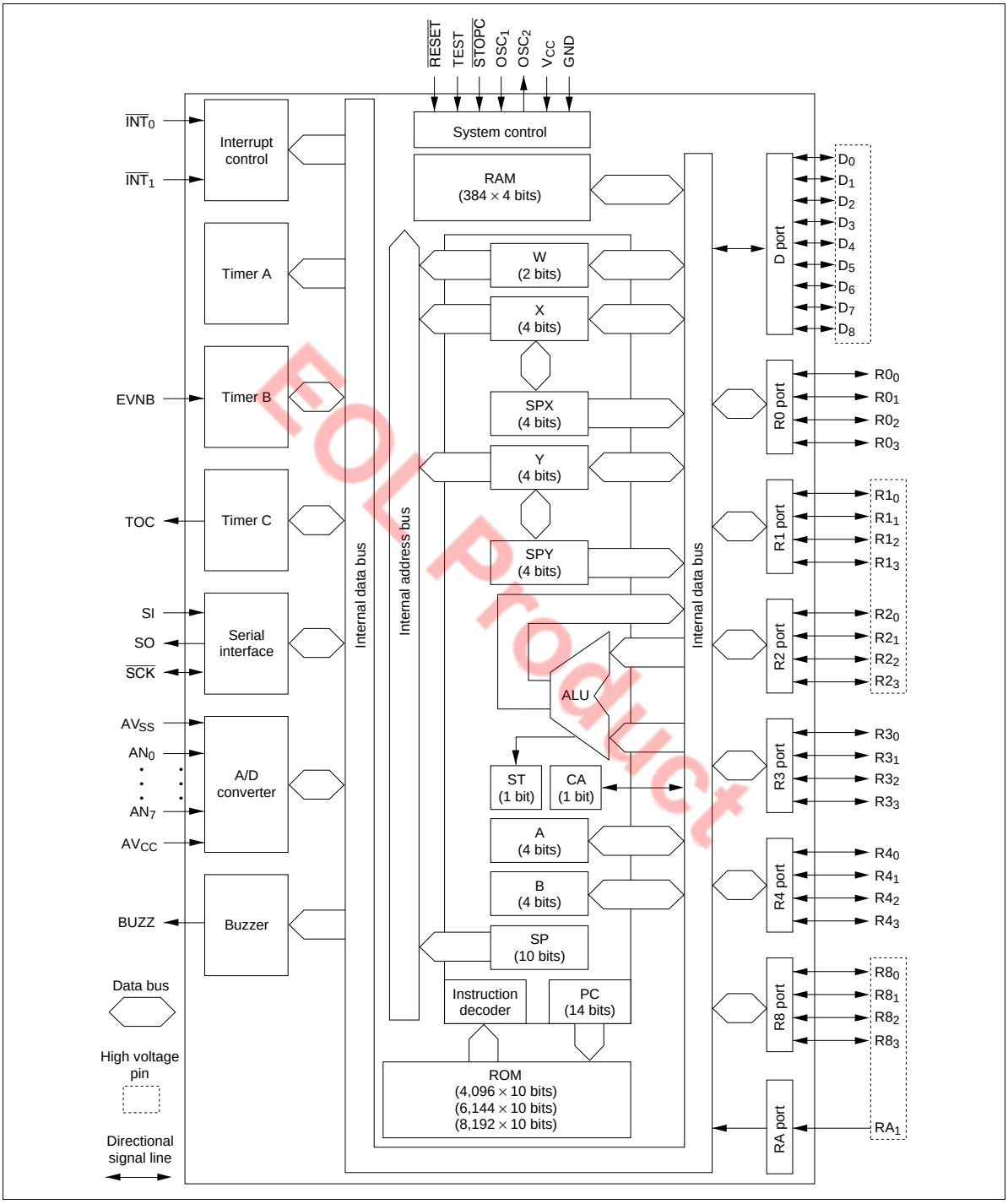
The HD4074318 is a PROM version of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

Pin Number		MCU Mode		PROM Mode	
DP-42S	**FP-44A**	**Pin**	**I/O**	**Pin**	**I/O**
1	39	RA_1/V_{disp}	I		
2	40	$R0_0/\overline{SCK}$	I/O	V_{CC}	
3	41	$R0_1$/SI	I/O	V_{CC}	
4	42	$R0_2$/SO	I/O		
5	43	$R0_3$/TOC	I/O		
6	1	TEST	I	V_{PP}	
7	2	$\overline{RESET}$	I	$\overline{RESET}$	I
8	3	OSC_1	I	V_{CC}	
9	4	OSC_2	O		
10	5	GND		GND	
11	6	AV_{SS}		GND	
12	7	$R3_0/AN_0$	I/O	O_0	I/O
13	8	$R3_1/AN_1$	I/O	O_1	I/O
14	9	$R3_2/AN_2$	I/O	O_2	I/O
15	10	$R3_3/AN_3$	I/O	O_3	I/O
16	11	$R4_0/AN_4$	I/O	O_4	I/O
17	12	$R4_1/AN_5$	I/O	O_5	I/O
18	13	$R4_2/AN_6$	I/O	O_6	I/O
19	14	$R4_3/AN_7$	I/O	O_7	I/O
20	15	AV_{CC}		V_{CC}	
21	16	V_{CC}		V_{CC}	
22	17	$D_0/\overline{INT}_0$	I/O	M_0	I
23	18	$D_1/\overline{INT}_1$	I/O	M_1	I
24	19	D_2/EVNB	I/O	A_1	I
25	20	D_3/BUZZ	I/O	A_2	I
26	21	$D_4/\overline{STOPC}$	I/O		
27	23	D_5	I/O	A_3	I
28	24	D_6	I/O	A_4	I
29	25	D_7	I/O	A_9	I
30	26	D_8	I/O	V_{CC}	

Pin Number		MCU Mode		PROM Mode	
DP-42S	**FP-44A**	**Pin**	**I/O**	**Pin**	**I/O**
31	27	$R8_0$	I/O	$\overline{CE}$	I
32	28	$R8_1$	I/O	$\overline{OE}$	I
33	29	$R8_2$	I/O	A_{13}	I
34	30	$R8_3$	I/O	A_{14}	I
35	31	$R1_0$	I/O	A_5	I
36	32	$R1_1$	I/O	A_6	I
37	33	$R1_2$	I/O	A_7	I
38	34	$R1_3$	I/O	A_8	I
39	35	$R2_0$	I/O	A_0	I
40	36	$R2_1$	I/O	A_{10}	I
41	37	$R2_2$	I/O	A_{11}	I
42	38	$R2_3$	I/O	A_{12}	I

I/O: Input/output pin; I: Input pin; O: Output pin

Block Diagram



Memory Map

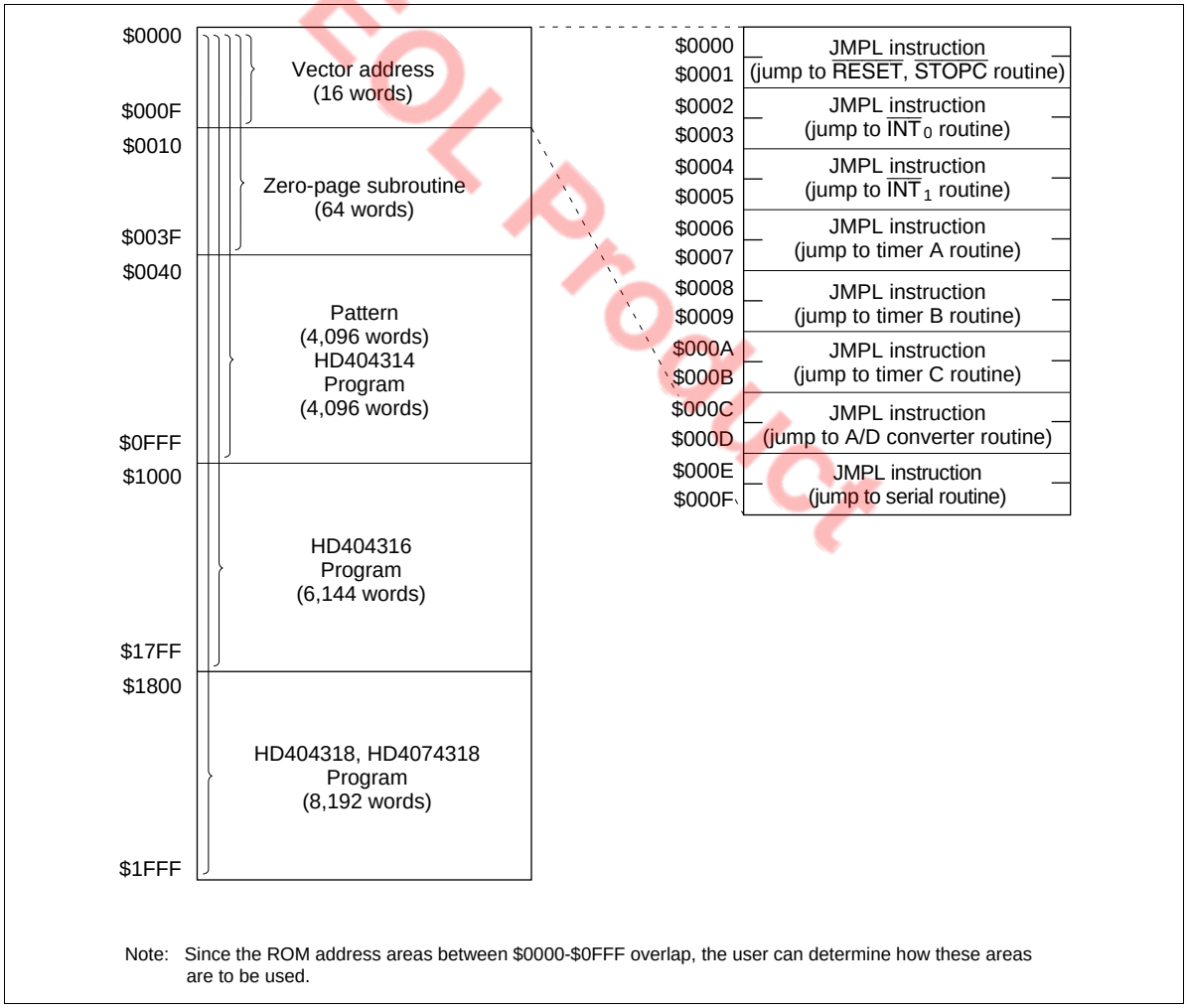
ROM Memory Map

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000–$0FFF (HD404314), $0000–$17FF (HD404316), $0000–$1FFF (HD404318, HD4074318)): The entire ROM area can be used for program coding.



Note: Since the ROM address areas between $0000-$0FFF overlap, the user can determine how these areas are to be used.

Figure 1 ROM Memory Map

RAM MemoryMap

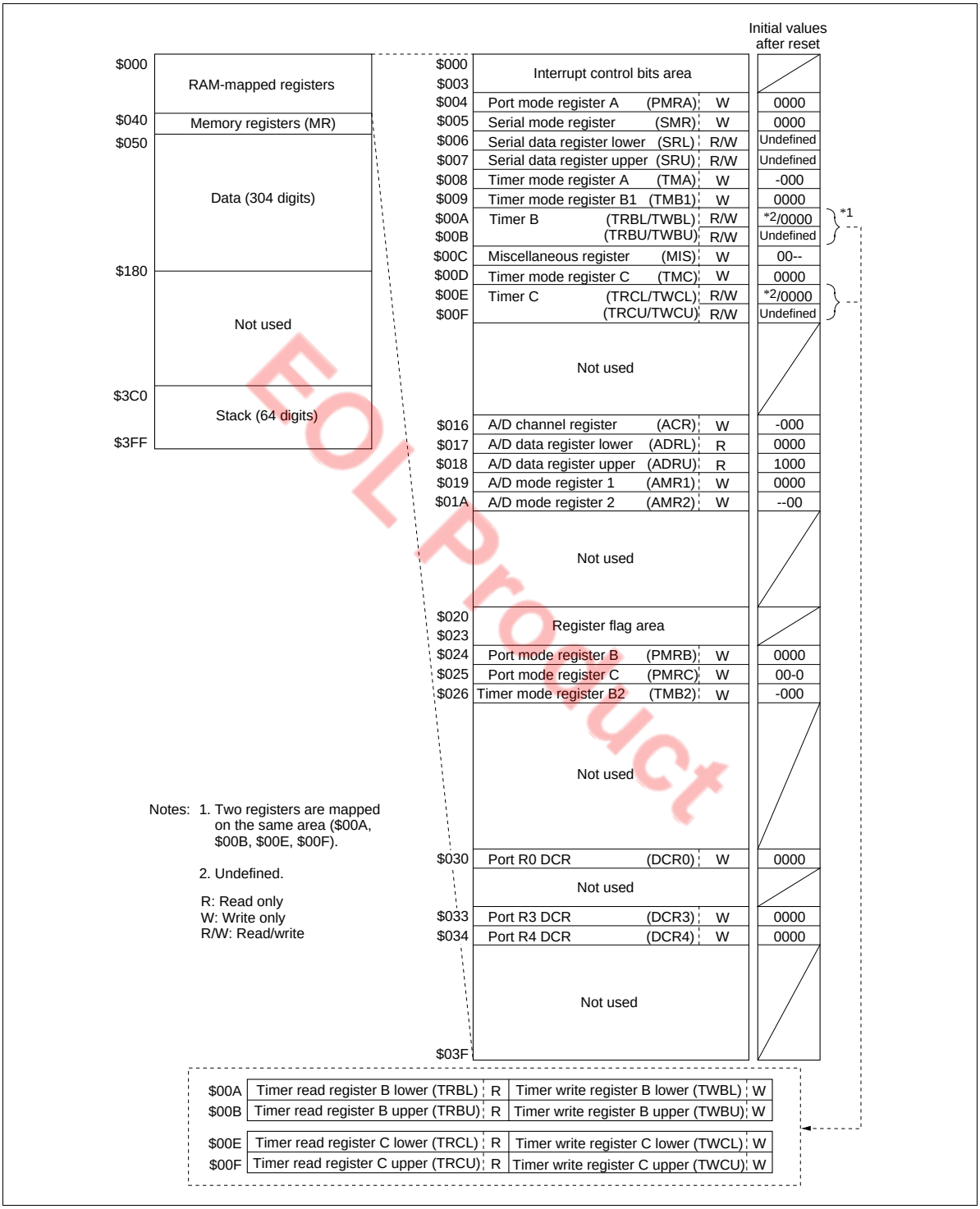


Figure 2 RAM Memory Map and Initial Values

Table 1 Initial Values of Flags after MCU Reset

Item		Initial Value
Interrupt flags/mask	Interrupt enable flag (IE)	0
	Interrupt request flag (IF)	0
	Interrupt mask (IM)	1
Bit registers	Watchdog timer on flag (WDON)	0
	A/D start flag (ADSF)	0
	Input capture status flag (ICSF)	0
	Input capture error flag (ICEF)	0
	I_{AD} off flag (IAOF)	0
	RAM enable flag (RAME)	0

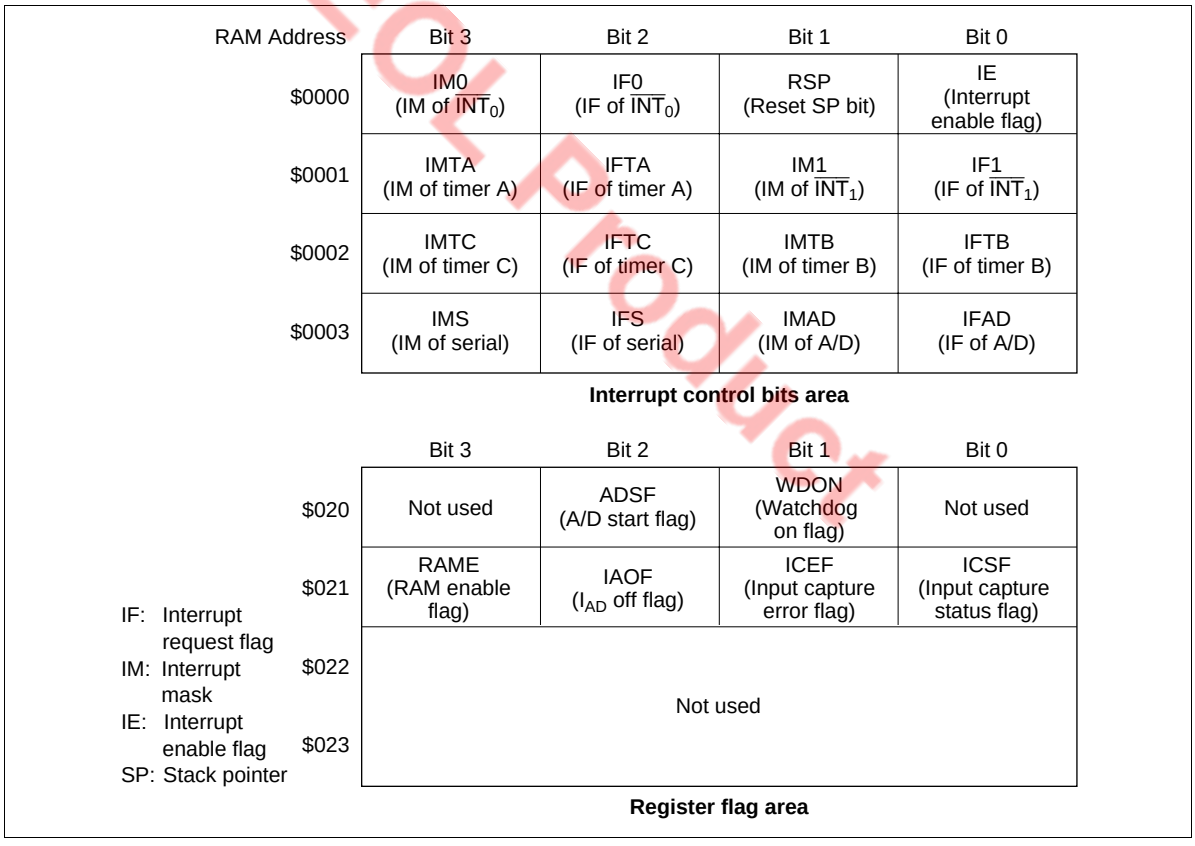
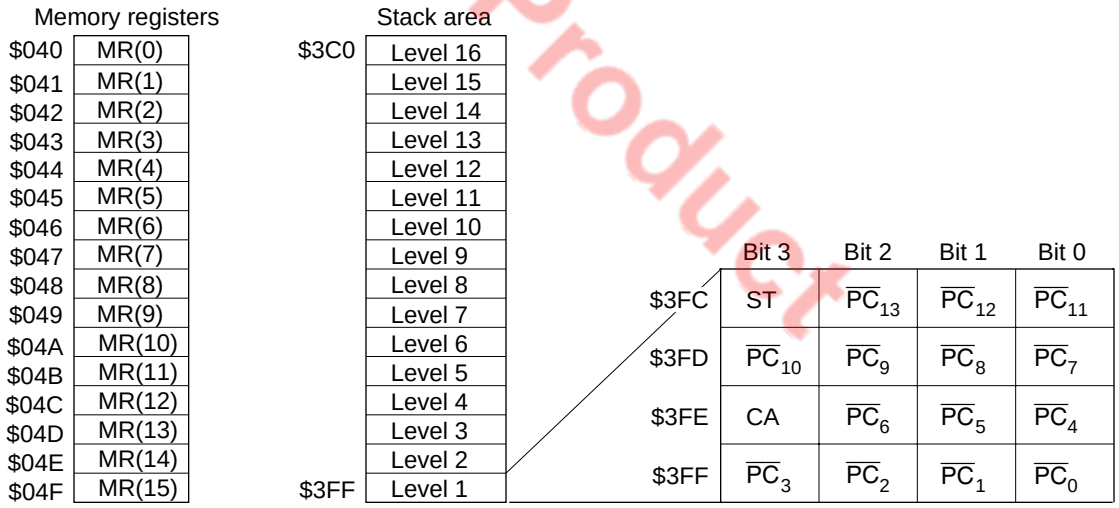


Figure 3 Interrupt Control Bits and Register Flag Areas Configuration

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
IAOF			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
ADSF	Allowed	Inhibited	Allowed
Not used	Not executed	Not executed	Inhibited

Note: WDON is reset by MCU reset or by $\overline{\text{STOPC}}$ enable for stop mode cancellation. The REM or REMD instruction must not be executed for ADSF during A/D conversion. If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions



PC_{13}–PC_0 : Program counter
ST: Status flag
CA: Carry flag

Figure 5 Configuration of Memory Registers and Stack Area, and Stack Position

Registers and Flags

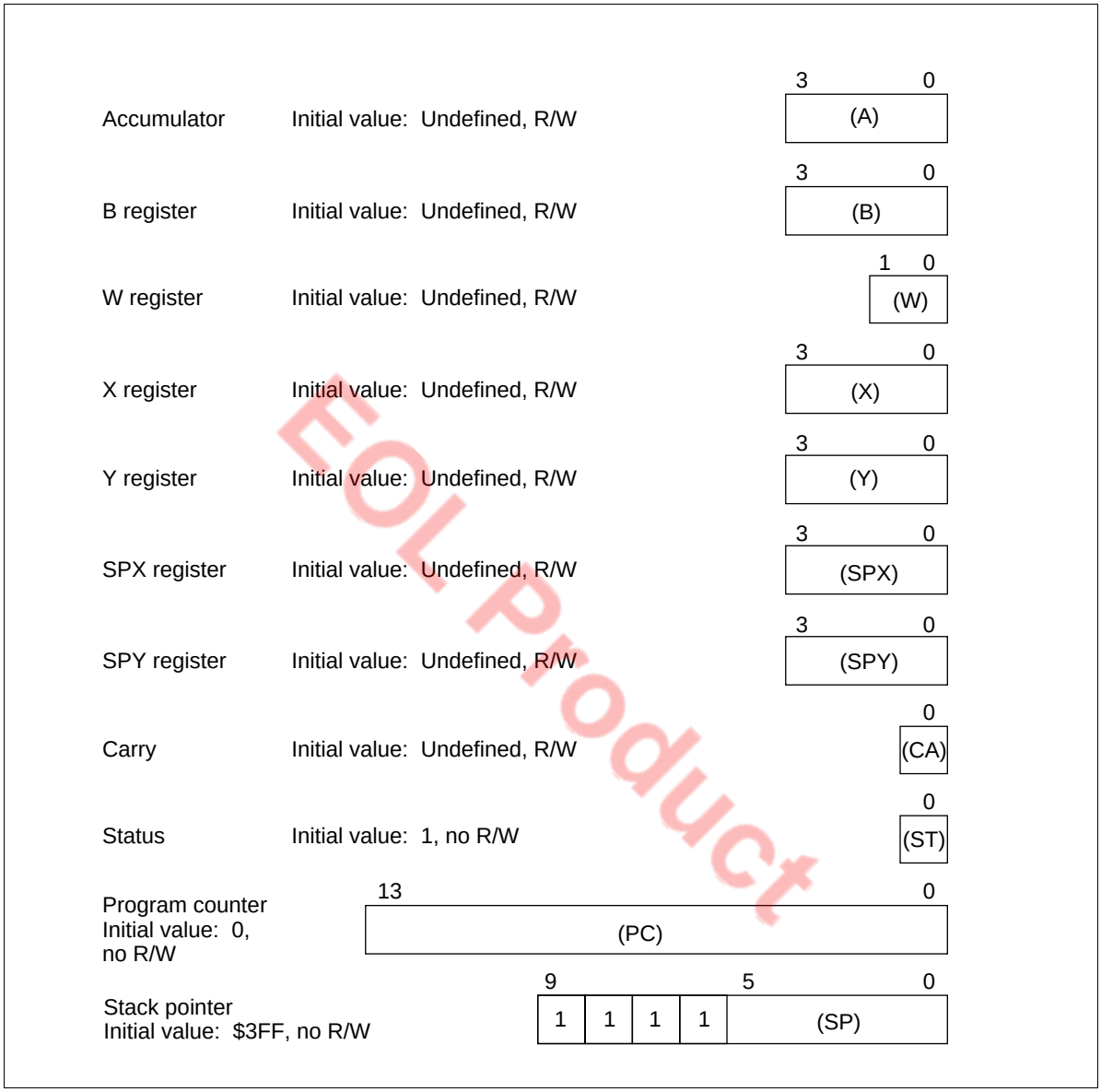


Figure 6 Registers and Flags

Addressing Modes

RAM Addressing Modes

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode (LAMR, XMRA): The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

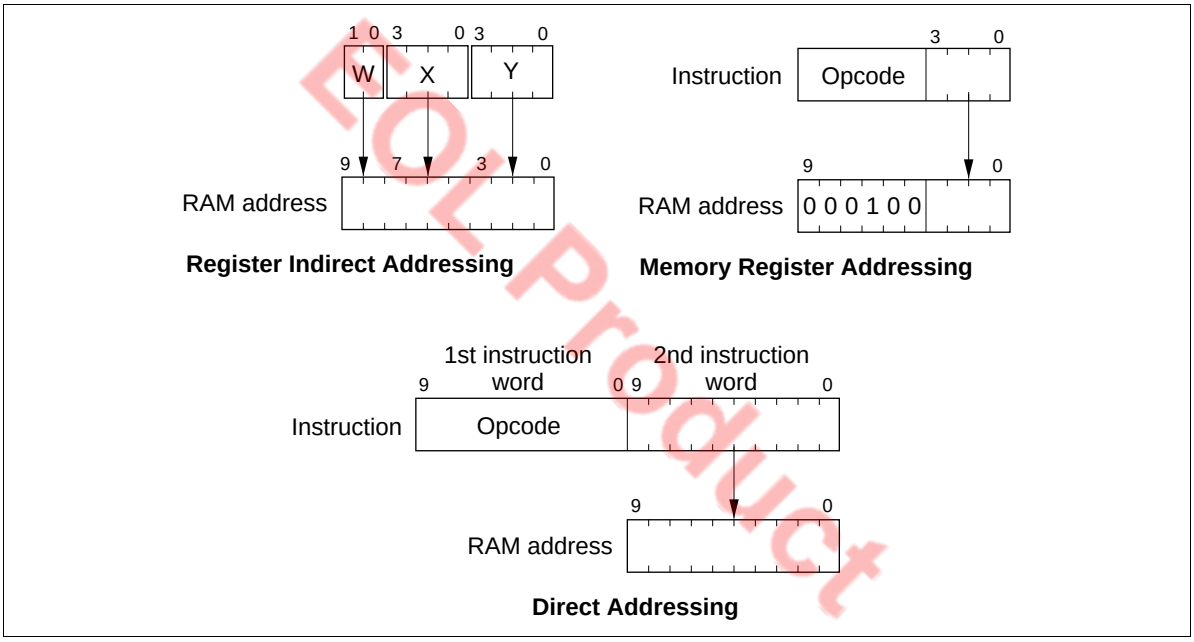


Figure 7 RAM Addressing Modes

ROM Addressing Modes

Direct Addressing Mode: A program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction.

Current Page Addressing Mode: A program can branch to any address in the current page (256 words per page) by executing the BR instruction.

Zero-Page Addressing Mode: A program can branch to any subroutine located in the zero-page subroutine area ($0000–$003F) by executing the CAL instruction.

Table Data Addressing Mode: A program can branch to an address determined by the contents of 4-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

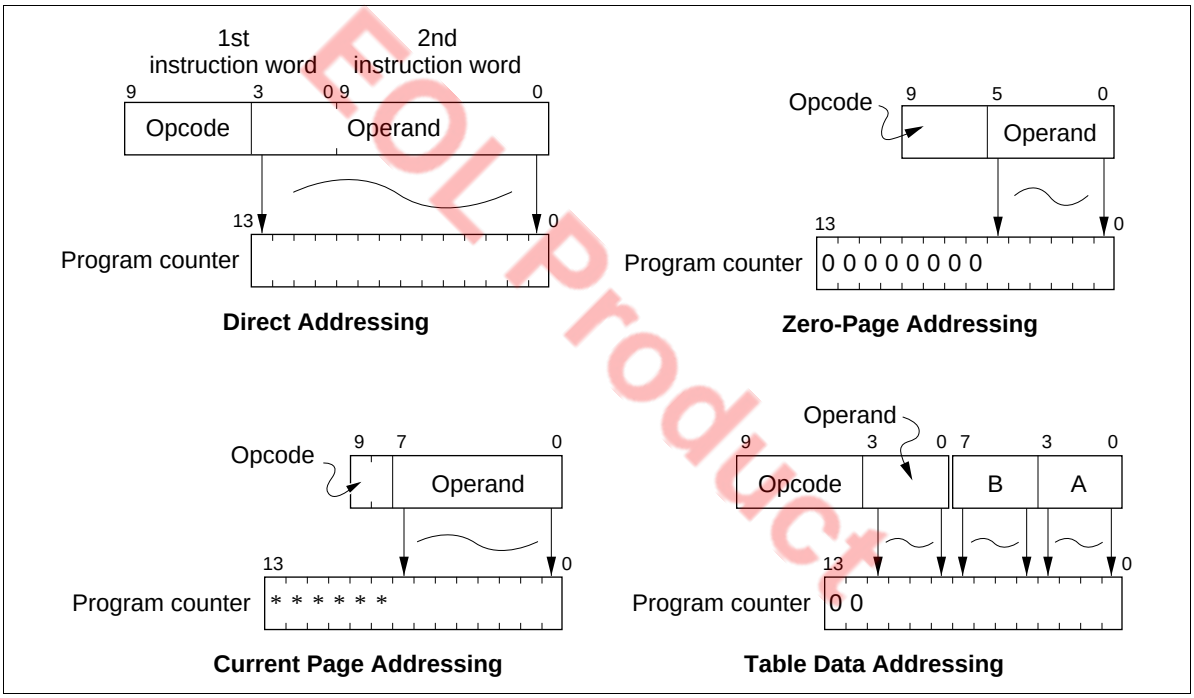


Figure 8 ROM Addressing Modes

Table 2 Instruction Set Classification

Instruction Type	Function	Number of Instructions
Immediate	Transferring constants to the accumulator, B register, and RAM.	4
Register-to-register	Transferring contents of the B, Y, SPX, SPY, or memory registers to the accumulator	8
RAM addressing	Available when accessing RAM in register indirect addressing mode	13
RAM register	Transferring data between the accumulator and memory.	10
Arithmetic	Performing arithmetic operations with the contents of the accumulator, B register, or memory.	25
Compare	Comparing contents of the accumulator or memory with a constant	12
RAM bit manipulation	Bit set, bit reset, and bit test.	6
ROM addressing	Branching and jump instructions based on the status condition.	8
Input/output	Controlling the input/output of the R and D ports; ROM data reference with the P instruction	11
Control	Controlling the serial communication interface and low-power dissipation modes.	4
		Total: 101 instructions

Interrupts

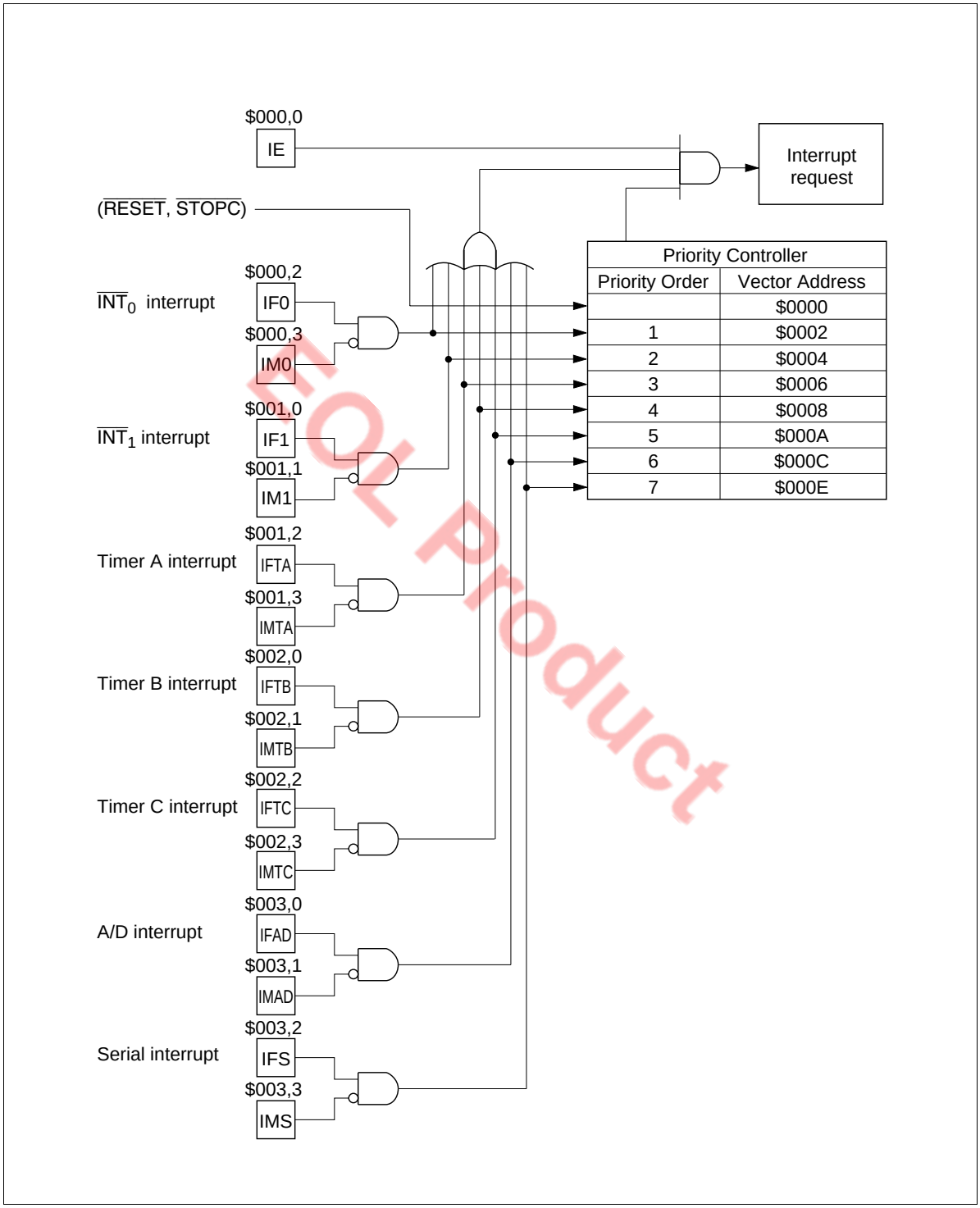


Figure 9 Interrupt Control Circuit

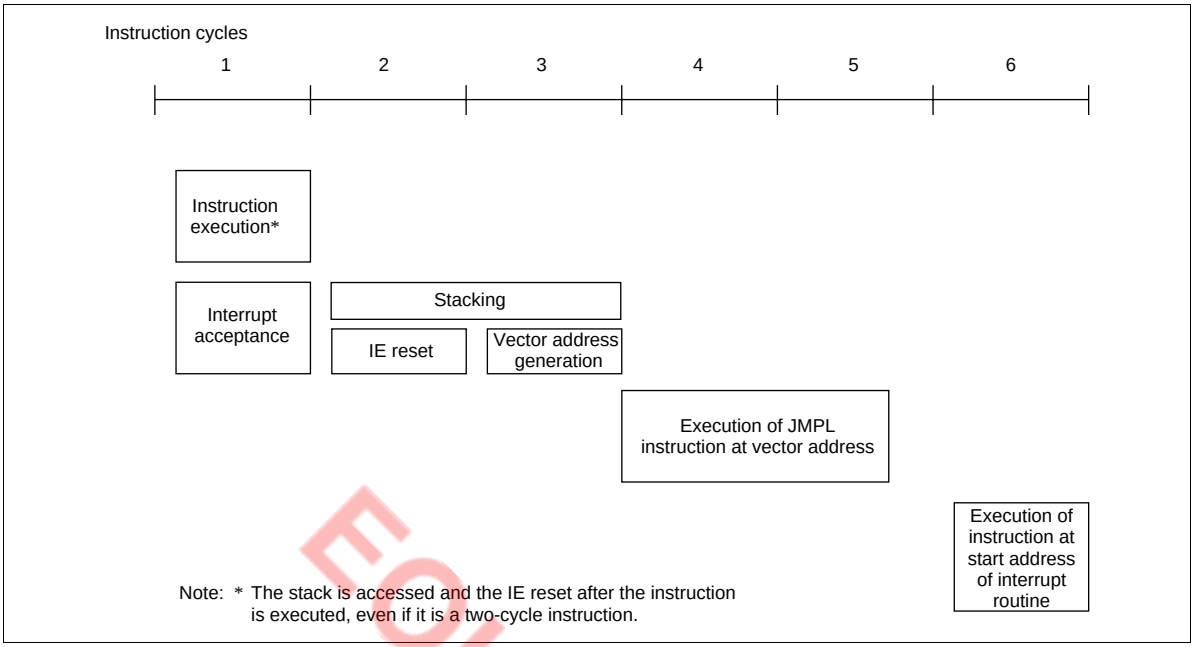


Figure 10 Interrupt Processing Sequence

Operating Modes

The MCU has three operating modes as shown in table 3. Transitions between operating modes are shown in figure 11.

Table 3 Operations in Each Operating Mode

Function	Active Mode	Standby Mode	Stop Mode
System oscillator	OP	OP	Stopped
CPU	OP	Retained	Reset
RAM	OP	Retained	Retained
Timer A	OP	OP	Reset
Timers B, C	OP	OP	Reset
Serial interface	OP	OP	Reset
A/D	OP	OP	Reset
I/O	OP	Retained	Reset

Note: OP implies in operation

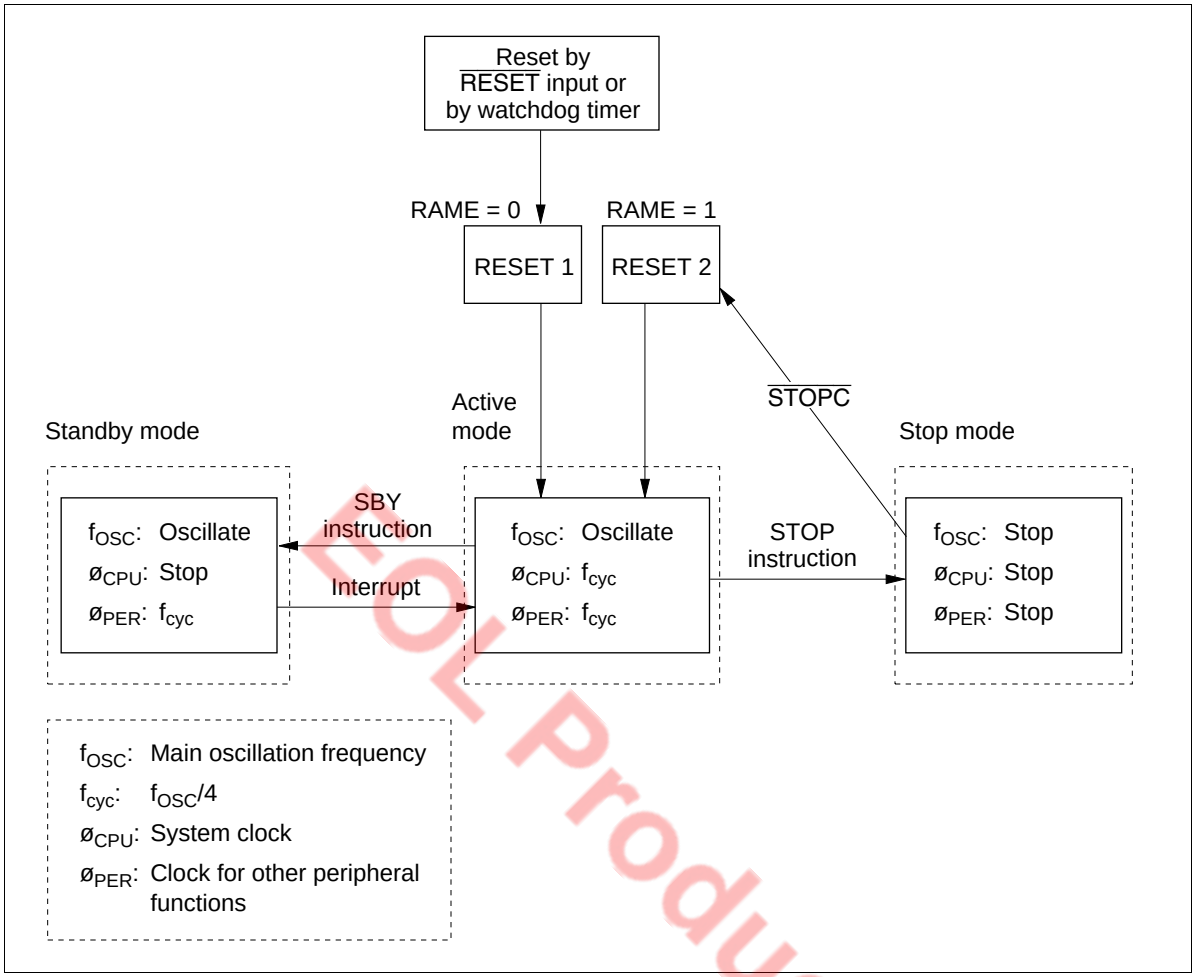


Figure 11 MCU Status Transitions

In stop mode, the system oscillator is stopped. To ensure a proper oscillation stabilization period of at least t_{RC} when clearing stop mode, execute the cancellation according to the timing chart in figure12.

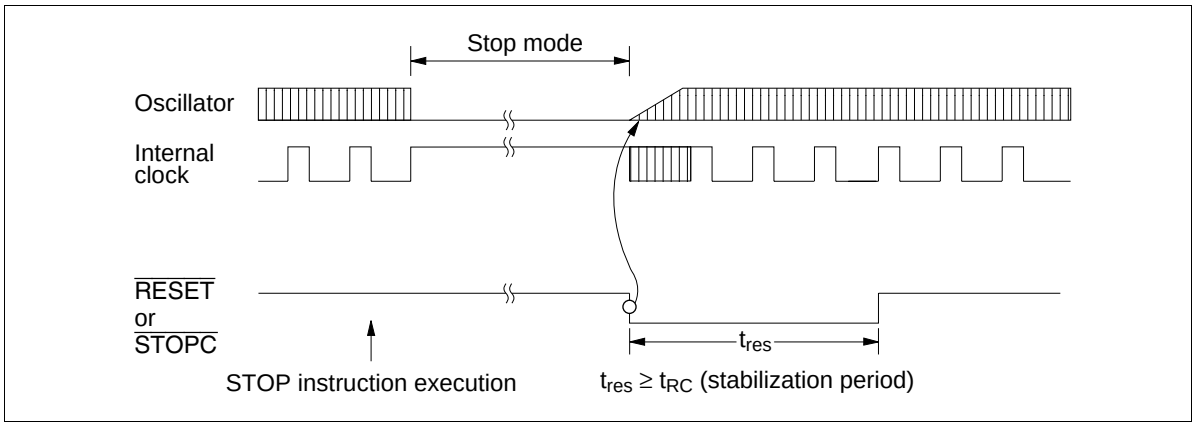


Figure 12 Timing of Stop Mode Cancellation

MCU Operation Sequence: The MCU operates in the sequence shown in figure 13 and figure 14.
The low-power mode operation sequence is shown in figure 14. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

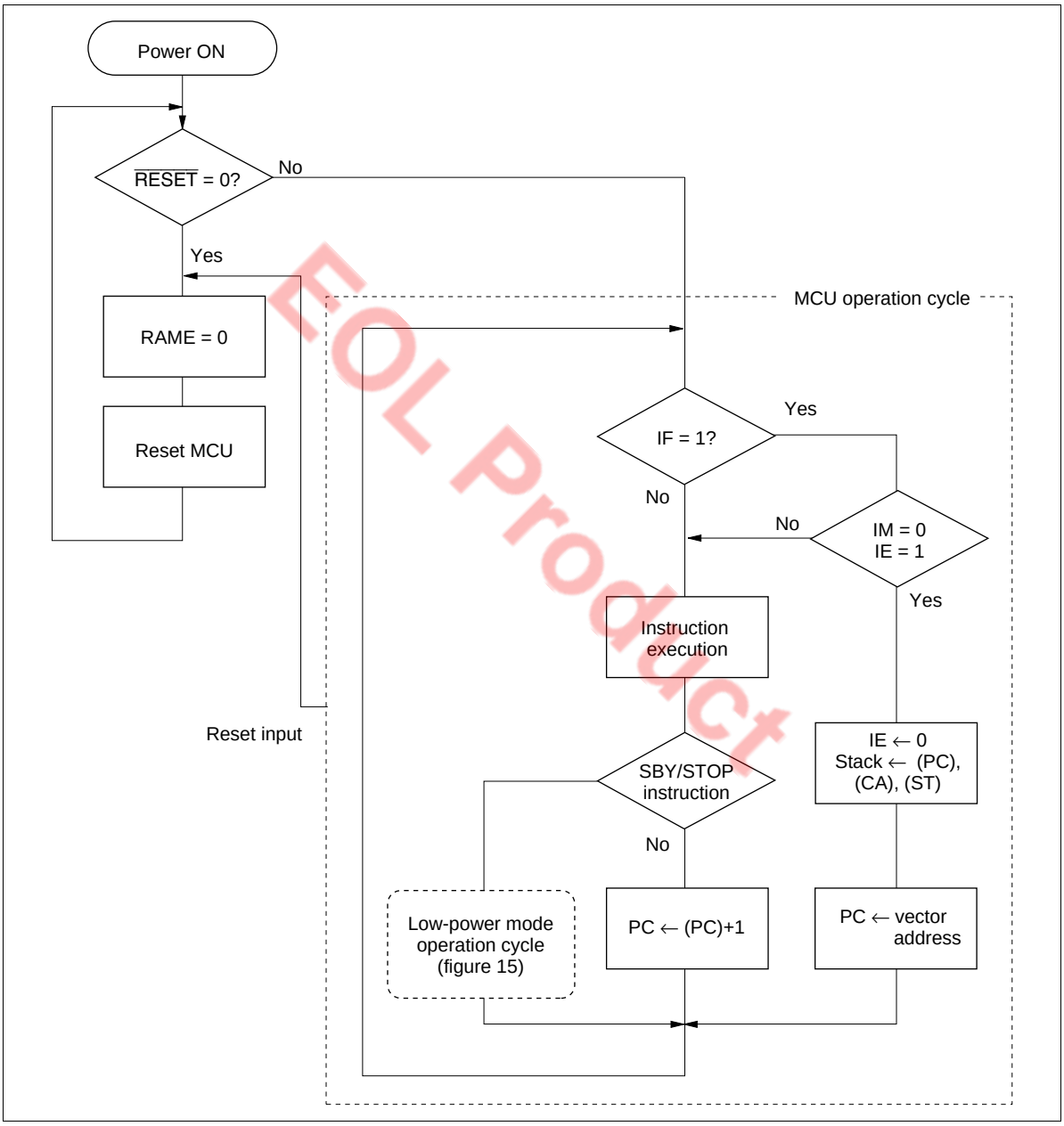


Figure 13 MCU Operating Sequence (Power ON)

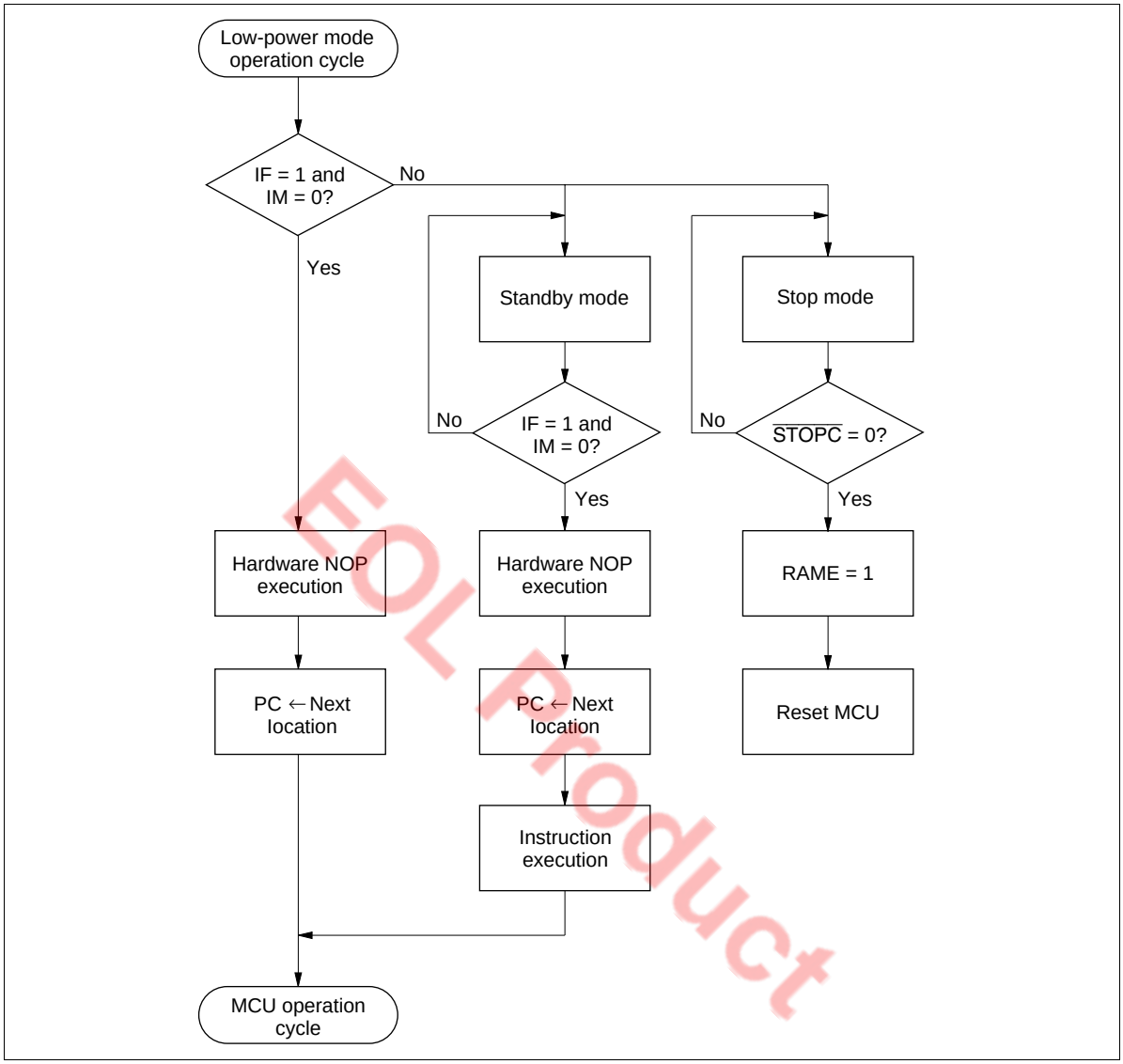


Figure 14 MCU Operating Sequence (Low-Power Mode Operation)

Oscillator Circuit

Figure 15 shows a block diagram of the clock generation circuit.

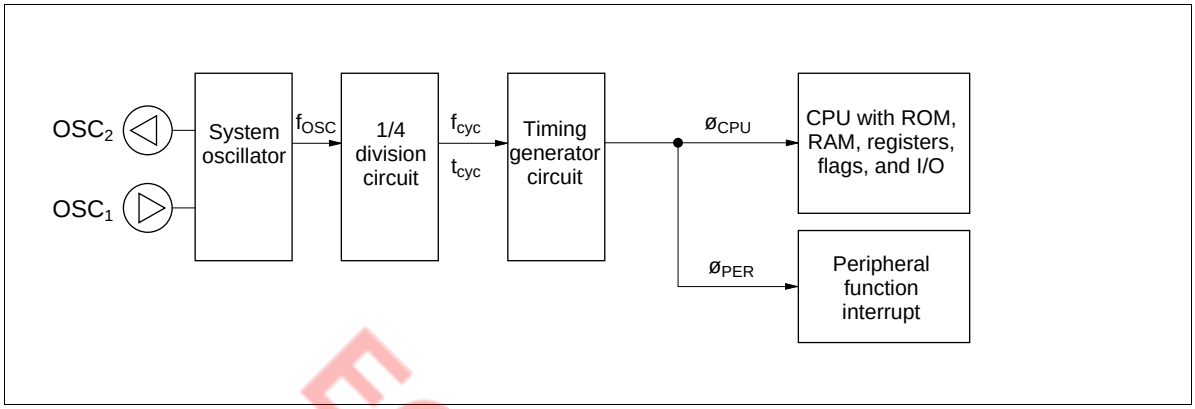


Figure 15 Clock Generation Circuit

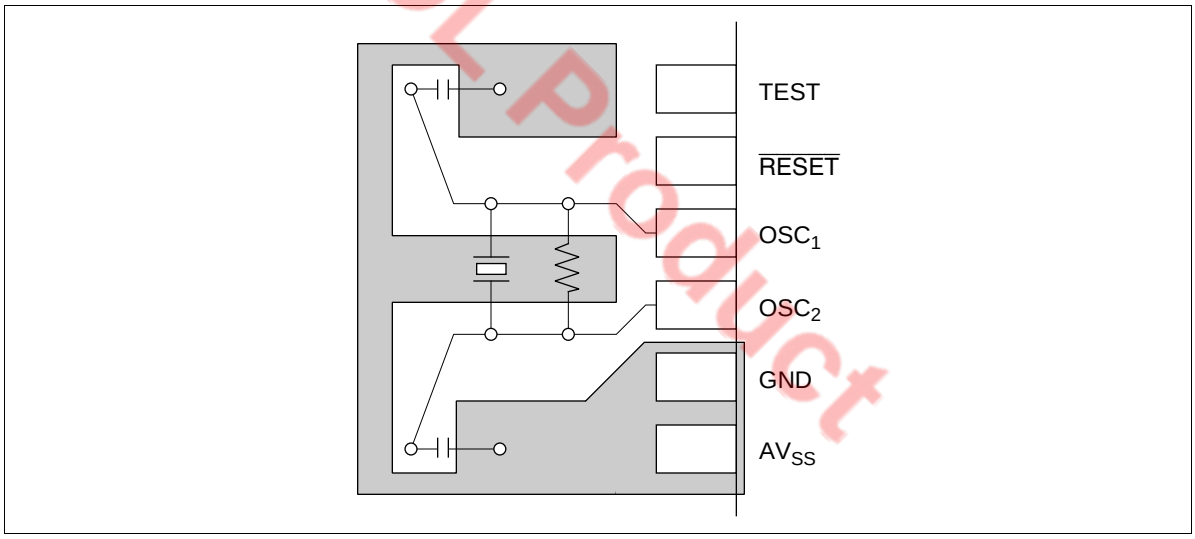
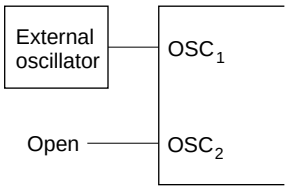
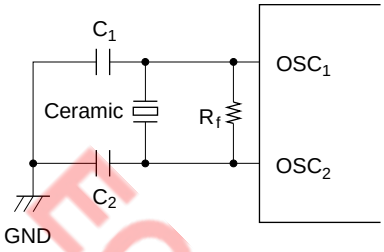
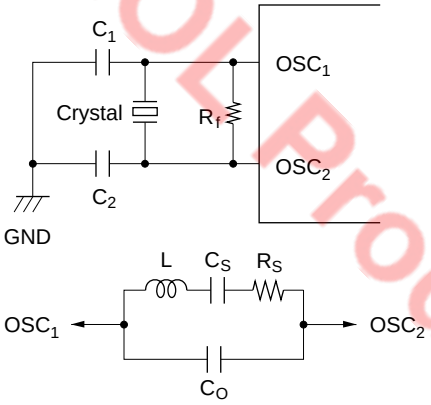


Figure 16 Typical Layout of Crystal and Ceramic Oscillator

Table 4 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ ±20% $C_1 = C_2$ = 30 pF ±20%
Crystal oscillator (OSC_1, OSC_2)		R_f = 1 MΩ ±20% $C_1 = C_2$ = 10 to 22 pF ±20% Crystal: Equivalent to circuit shown below C_0 = 7 pF max. R_S = 100 Ω max.

Notes: 1. Since the circuit constants change depending on the crystal or ceramic oscillator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and elements should be as short as possible, and must not cross other wiring (see figure 16).

I/O Ports

The MCU has 33 input/output pins (D_0–D_8, R0–R4, R8) and one input-only pin (RA_1). The following describes the features of the I/O ports.

- The 21 pins consisting of D_0–D_8, R1, R2, and R8 are all high-voltage I/O pins. RA_1 is a high-voltage input-only pin. These high-voltage pins can be equipped with or without pull-down resistance, as selected by the mask option.
- All standard output pins are CMOS output pins. However, the $R0_2$/SO pin can be programmed for NMOS open-drain output.
- In stop mode, input/output pins go to the high-impedance state
- All standard input/output pins have pull-up MOS built in, which can be individually turned on or off by software

Table 5 Control of Standard I/O Pins by Program

MIS3 (bit 3 of MIS)		**0**				**1**			
DCR		**0**		**1**		**0**		**1**	
PDR		**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off.

Data control register (DCR0: $030, DCR3: $033, DCR4: $034)

DCR0, DCR3, DCR4

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCR03, DCR33, DCR43,	DCR02, DCR32, DCR42,	DCR01, DCR31, DCR41,	DCR00, DCR30, DCR40

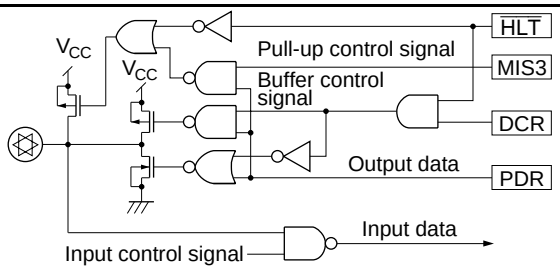
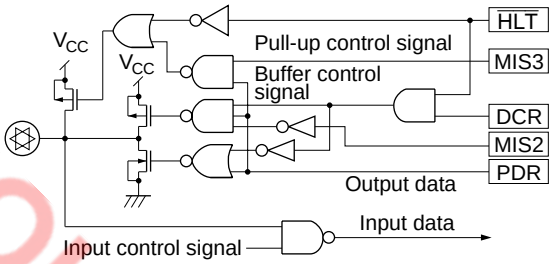
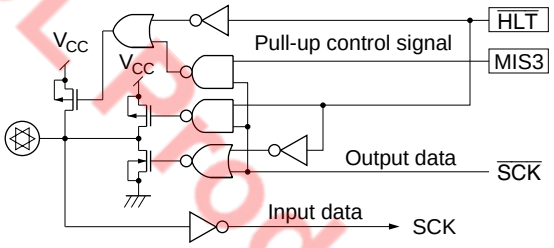
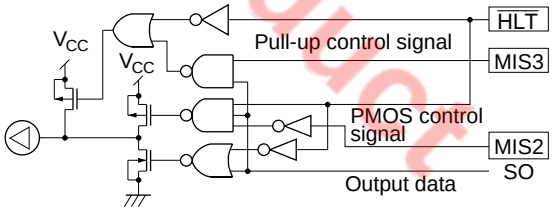
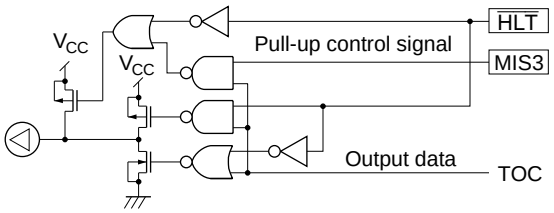
Bits 0 to 3	CMOS Buffer Control
0	CMOS buffer off (high impedance)
1	CMOS buffer on

Correspondence between ports and DCR bits

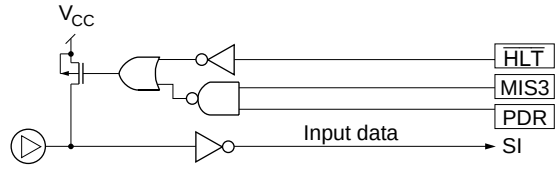
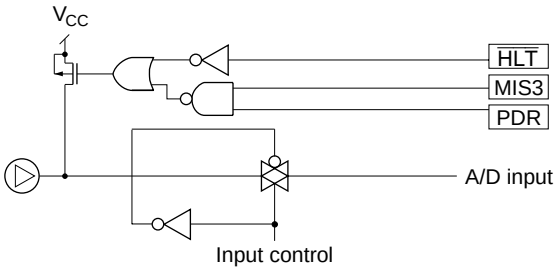
Register	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$

Figure 17 Data Control Register (DCR)

Table 6 Circuit Configurations of Standard I/O Pins

I/O Pin Type		Circuit	Pins
Input/output pins			$R0_0$, $R0_1$, $R0_3$ $R3_0$–$R3_3$, $R4_0$–$R4_3$
			$R0_2$
Peripheral function pins	Input/ output pins		$\overline{SCK}$
	Output pins		SO
			TOC

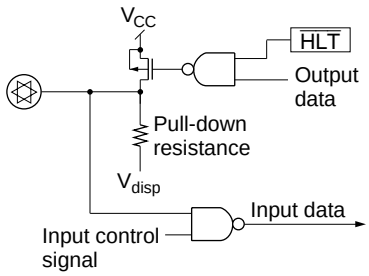
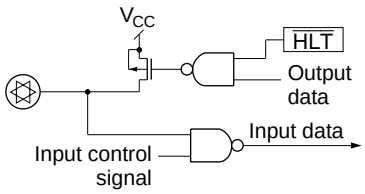
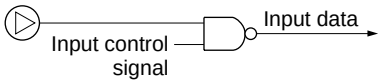
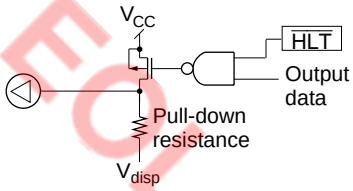
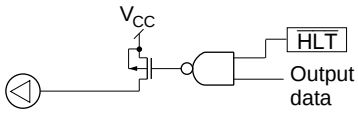
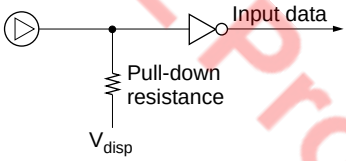
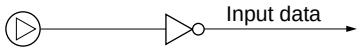
Notes on next page.

I/O Pin Type		Circuit	Pins
Peripheral function pins	Input/ pins		SI
			AN_0–AN_7

Notes: 1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The $\overline{HLT}$ signal goes low, and input/output pins the enter high-impedance state.

2. The $\overline{HLT}$ signal is 1 in active and standby modes.

Table 7 Circuit Configurations for High-Voltage Input/Output Pins

I/O Pin Type		With Pull-Down Resistance	Without Pull-Down Resistance	Pins
Input/output pins				D_0–D_8, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R8_0$–$R8_3$
Input pins				RA_1
Peripheral function pins	Output pins			BUZZ
	Input pins			$\overline{INT}_0$, $\overline{INT}_1$, EVNB, $\overline{STOPC}$

Notes: 1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The $\overline{HLT}$ signal goes low, and input/output pins the enter high-impedance state.
2. The $\overline{HLT}$ signal is 1 in active and standby modes.
3. The circuits of HD4074318 are without pull-down resistance.

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA3	D_3/BUZZ Mode Selection
0	D_3
1	BUZZ

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 18 Port Mode Register A (PMRA)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3*	PMRB2	PMRB1	PMRB0

PMRB2	D_2/EVNB Mode Selection
0	D_2
1	EVNB

PMRB3	D_4/$\overline{\text{STOPC}}$ Mode Selection
0	D_4
1	$\overline{\text{STOPC}}$

PMRB0	D_0/$\overline{\text{INT}}_0$ Mode Selection
0	D_0
1	$\overline{\text{INT}}_0$

PMRB1	D_1/$\overline{\text{INT}}_1$ Mode Selection
0	D_1
1	$\overline{\text{INT}}_1$

Note: * PMRB3 is reset to 0 only by RESET input. When STOPC is input in stop mode, PMRB3 is not reset but retains its value.

Figure 19 Port Mode Register B (PMRB)

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	MIS3	MIS2	Not used	Not used

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on (refer to table 5)

MIS2	CMOS Buffer On/Off Selection for Pin $R0_2$/SO
0	CMOS on
1	CMOS off

Note: The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

Figure 20 Miscellaneous Register (MIS)

Prescaler

The MCU has a built-in prescaler labeled as prescaler S (PSS), which divides the system clock and then outputs divided clock signals to the peripheral function modules, as shown in figure21.

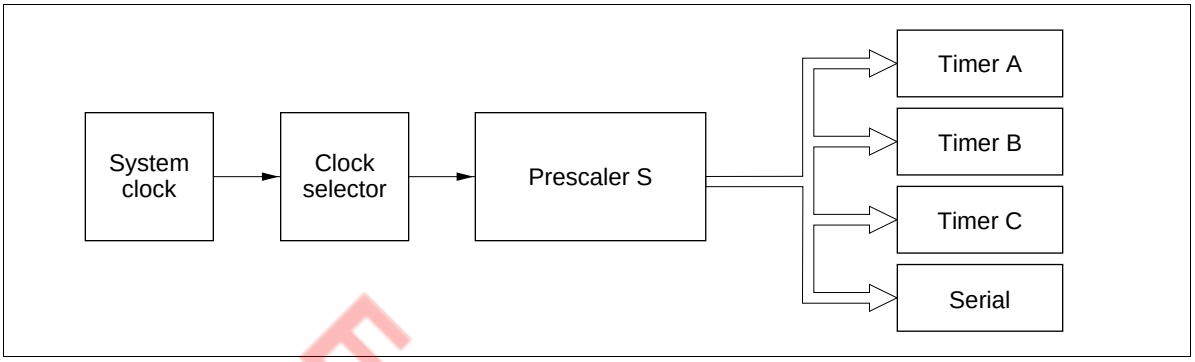


Figure 21 Prescaler Output Supply

Timers

The MCU has three built-in timers: A, B, and C. The functions of each timer are listed in table 7.

Timer A

Timer A is an 8-bit free-running timer that has the following features:

- One of eight internal clocks can be selected from prescaler S according to the setting of timer mode register A (TMA: $008)
- An interrupt request can be generated when timer counter A (TCA) overflows
- Input clock frequency must not be modified during timer A operation

Table 7 Timer Functions

Functions		Timer A	Timer B	Timer C
Clock source	Prescaler S	Available	Available	Available
	External event	—	Available	—
Timer functions	Free-running	Available	Available	Available
	Event counter	—	Available	—
	Reload	—	Available	Available
	Watchdog	—	—	Available
	Input capture	—	Available	—
Timer output	PWM	—	—	Available

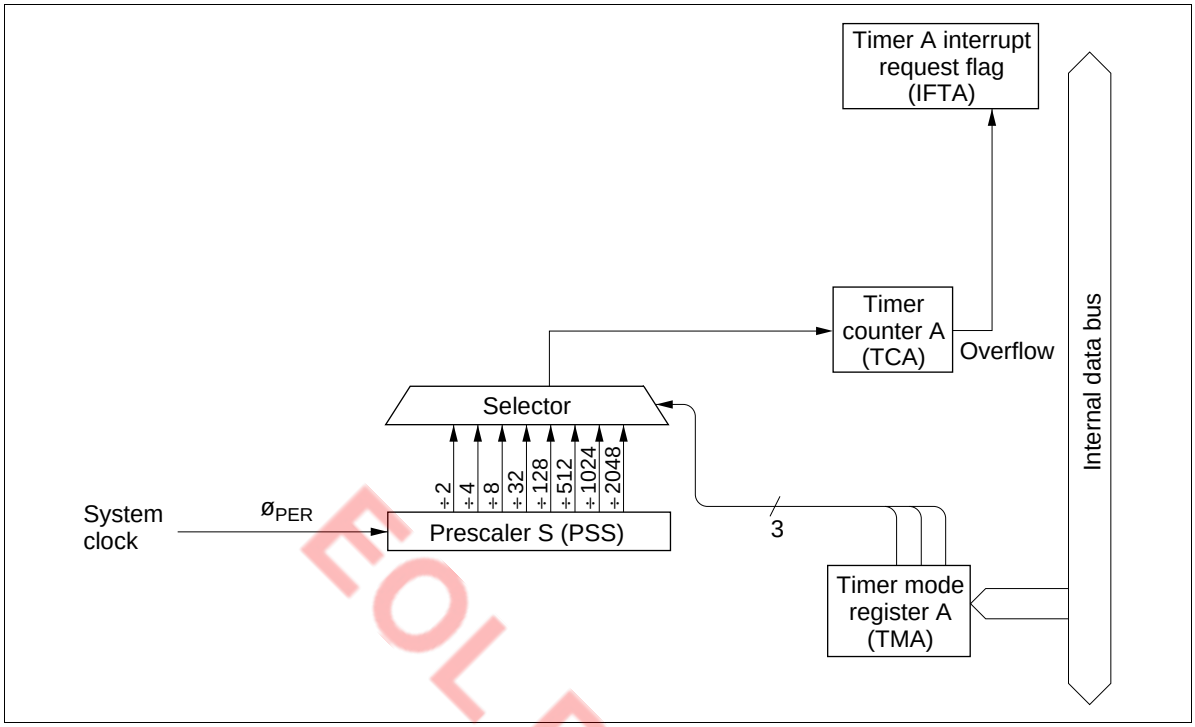


Figure 22 Timer A Block Diagram

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMA2	TMA1	TMA0

TMA2	TMA1	TMA0	Source Prescaler	Input clock frequency
0	0	0	PSS	$2048t_{cyc}$
		1	PSS	$1024t_{cyc}$
	1	0	PSS	$512t_{cyc}$
		1	PSS	$128t_{cyc}$
1	0	0	PSS	$32t_{cyc}$
		1	PSS	$8t_{cyc}$
	1	0	PSS	$4t_{cyc}$
		1	PSS	$2t_{cyc}$

Figure 23 Timer Mode Register A (TMA)

Timer B

Timer B is an 8-bit multifunction timer that includes free-running, reload, and input capture timer features. These are described as follows.

- By setting timer mode register B1 (TMB1: $009), one of seven internal clocks supplied from prescaler S can be selected, or timer B can be used as an external event counter
- By setting timer mode register B2 (TMB2: $026), detection edge type of EVNB can be selected
- By setting timer write register BL, BU (TWBL, BU: $00A, $00B), timer counter B (TCB) can be written to during reload timer operation
- By setting timer read register BL, BU (TRBL, BU: $00A, $00B), the contents of timer counter B can be read out
- Timer B can be used as an input capture timer to count the clock cycles between trigger edges input as an external event
- An interrupt can be requested when timer counter B overflows or when a trigger input edge is received during input capture operation

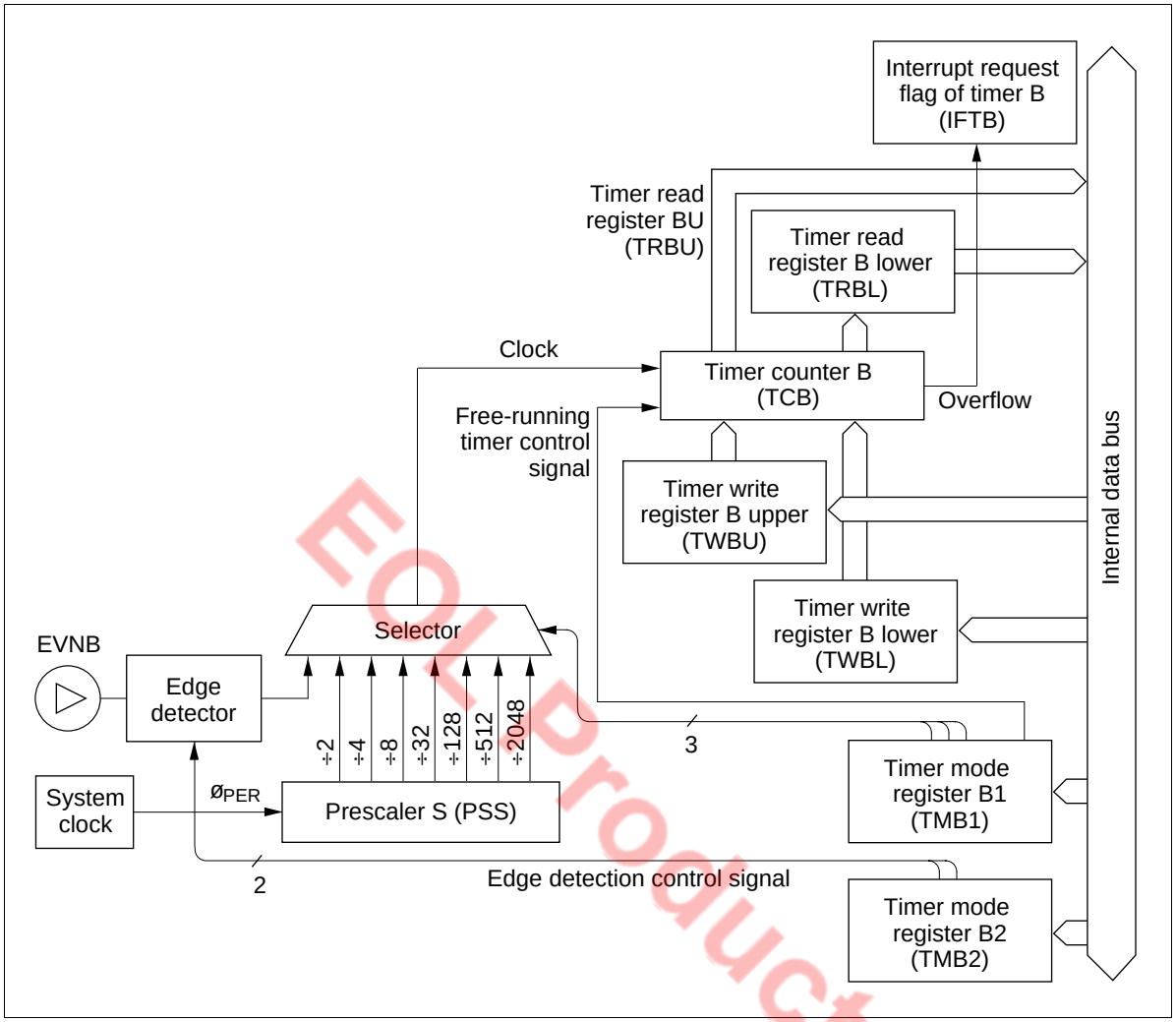


Figure 24 Timer B Free-Running and Reload Operation Block Diagram

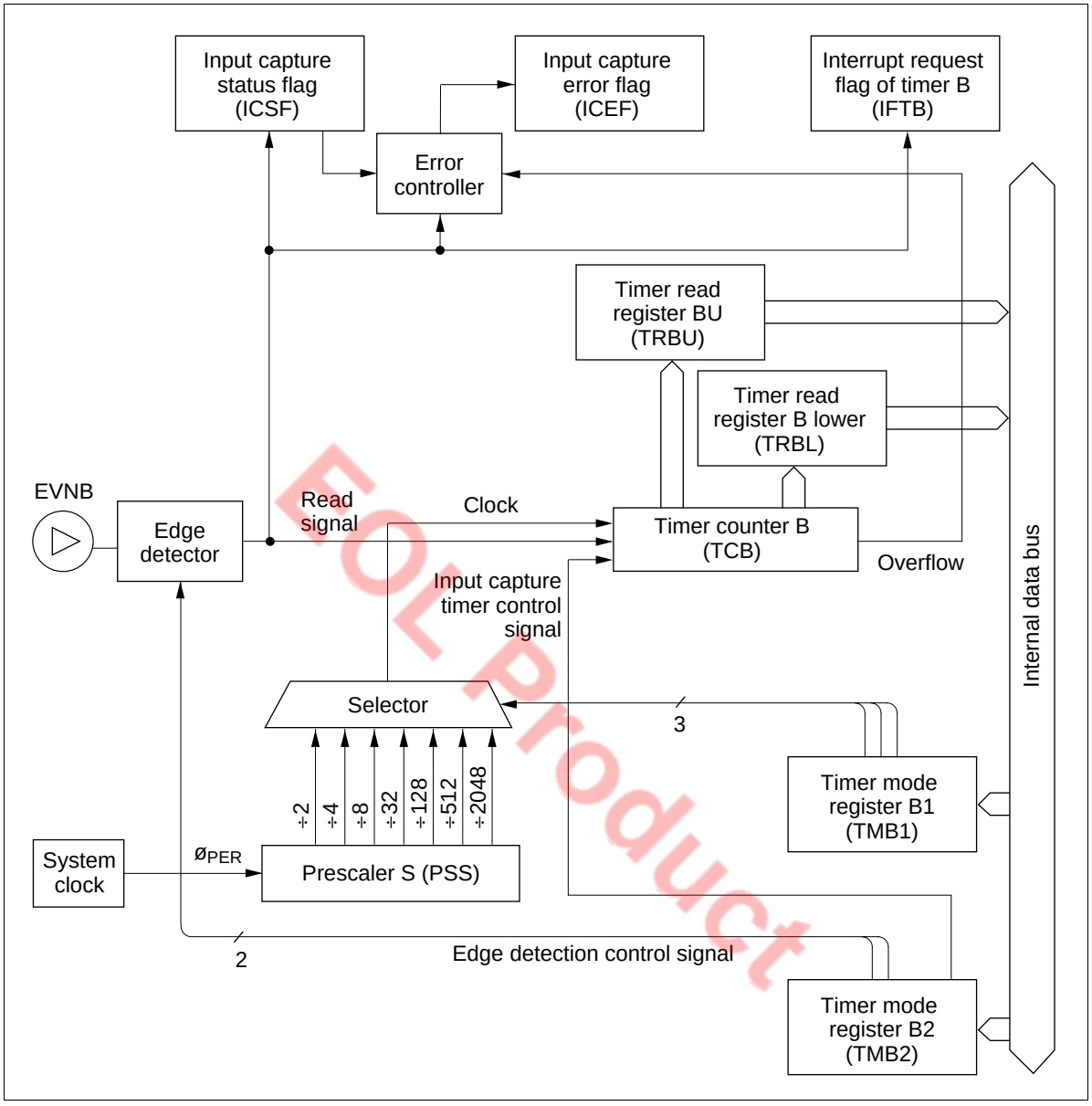


Figure 25 Timer B Input Capture Operation Block Diagram

Timer mode register B1 (TMB1: $009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input Clock Period and Input Clock Source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	D_2/EVNB (external event input)

Figure 26 Timer Mode Register B1 (TMB1)

Timer mode register B2 (TMB2: $026)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMB22	TMB21	TMB20

TMB21	TMB20	EVNB Edge Detection Selection
0	0	No detection
	1	Falling edge detection
1	0	Rising edge detection
	1	Rising and falling edge detection

TMB22	Free-Running/Reload and Input Capture Selection
0	Free-Running/Reload
1	Input capture

Figure 27 Timer Mode Register B2 (TMB2)

Timer C

Timer C is an 8-bit multifunction timer that includes free-running, reload, and watchdog timer features, which are described as follows.

- By setting timer mode register C (TMC: $00D), one of eight internal clocks supplied from prescaler S can be selected
- By selecting pin TOC with bit 2 (PMRA2) of port mode register A (PMRA: $004), timer C output (PWM output) is enabled
- By setting timer write register CL, CU (TWCL, CU: $00E, $00F), timer counter C (TCC) can be written to
- By setting timer read register CL, CU (TRCL, CU: $00E, $00F), the contents of timer counter C can be read out
- An interrupt can be requested when timer counter C overflows
- Timer counter C can be used as a watchdog timer for detecting runaway program

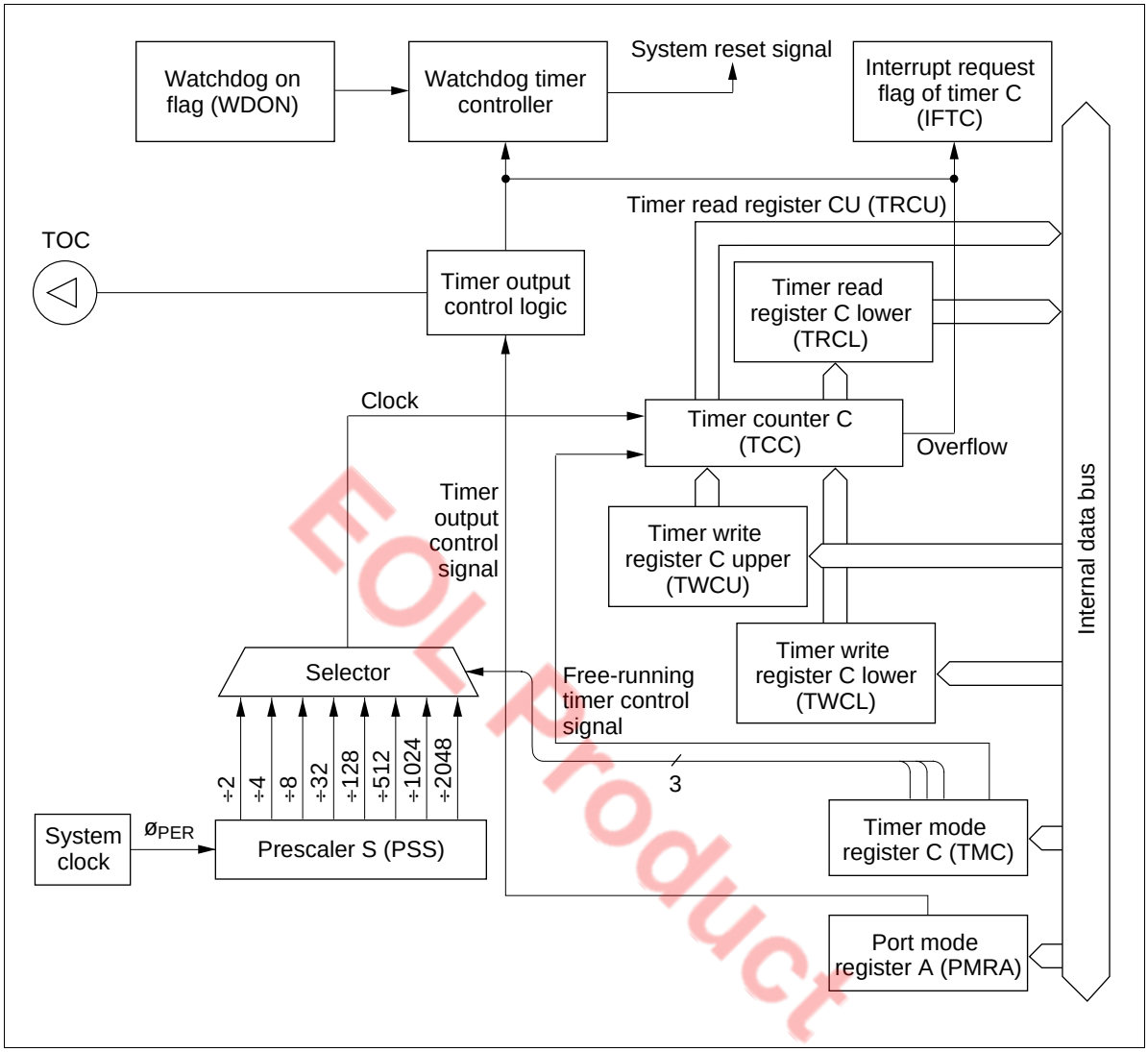


Figure 28 Timer C Block Diagram

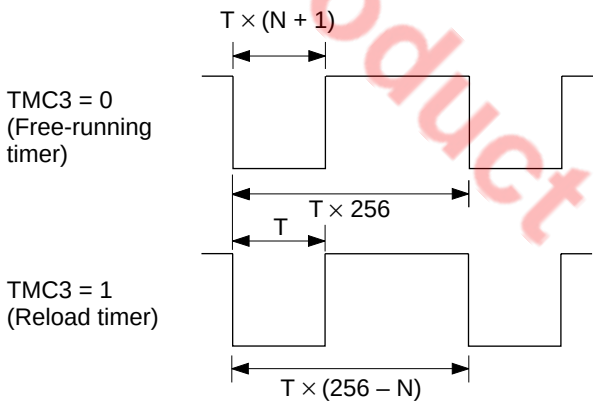
Timer mode register C (TMC: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC3	TMC2	TMC1	TMC0

TMC3	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMC2	TMC1	TMC0	Input Clock Period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 29 Timer Mode Register C (TMC)



Notes: T: Input clock period supplied to counter. (The clock source and system clock division ratio are determined by timer mode register C.)
N: Value of timer write register C. (When N = 255 ($FF), PWM output is fixed low.)

Figure 30 PWM Output Waveform

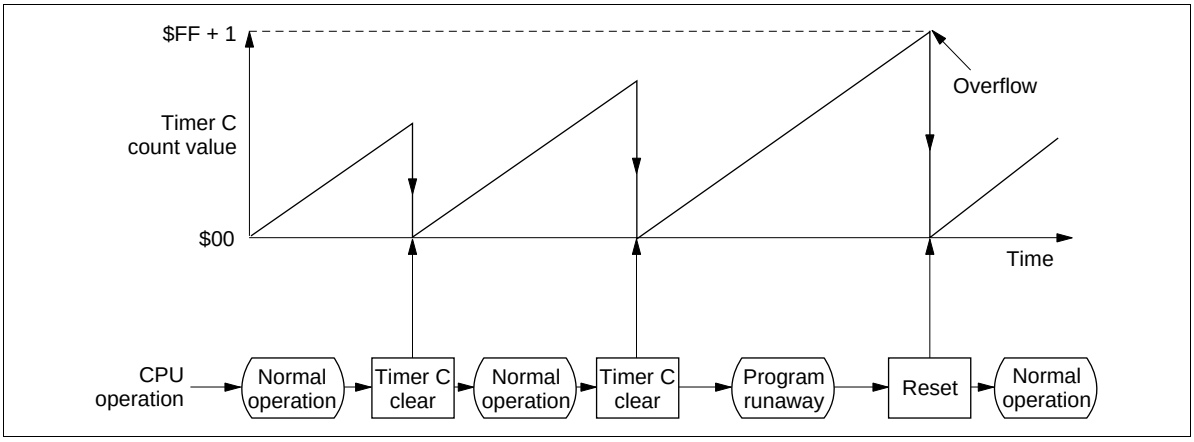
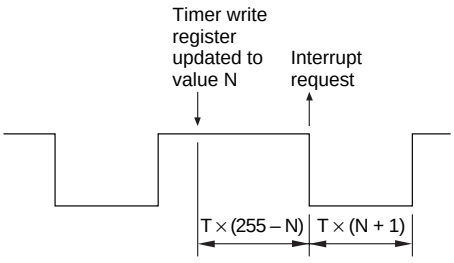
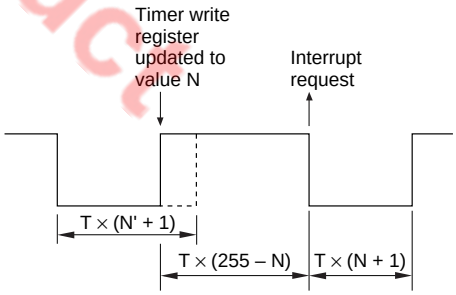
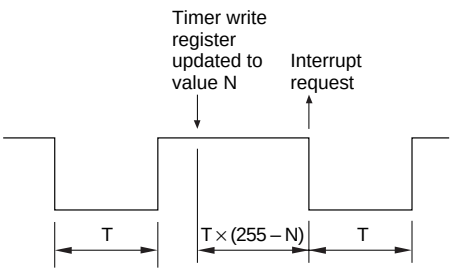
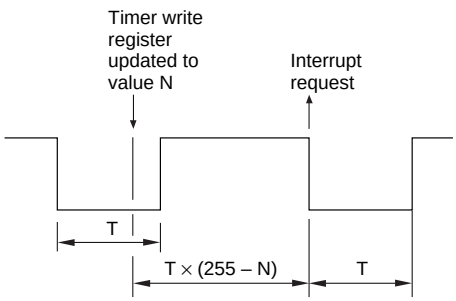


Figure 31 Watchdog Timer Operation Flowchart

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 8. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 8 PWM Output Following Update of Timer Write Register

	PWM Output	
Mode	Timer Write Register is Updated during High PWM Output	Timer Write Register is Updated during Low PWM Output
Free running		
Reload		

Alarm Output Function

The MCU has an alarm output function built in. By setting port mode register C (PMRC: $025), one of four alarm frequencies supplied from the PSS can be selected.

Table 9 Port Mode Register C

PMRC		
Bit 3	**Bit 2**	**System Clock Divisor**
0	0	÷ 2048
	1	÷ 1024
1	0	÷ 512
	1	÷ 256

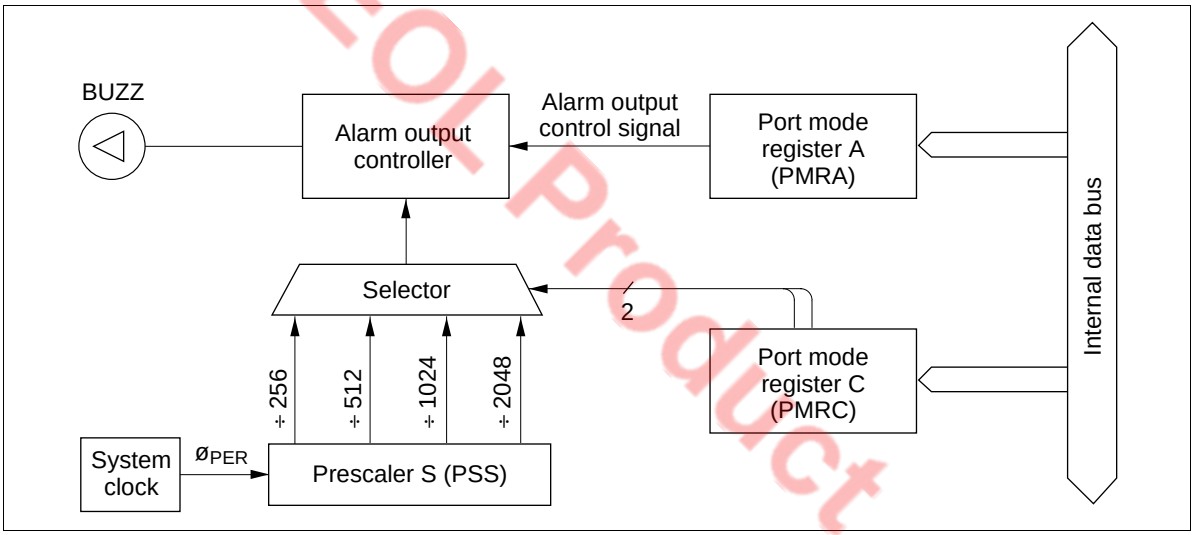


Figure 32 Alarm Output Function Block Diagram

Serial Interface

The MCU has a one-channel serial interface built in with the following features.

- One of 13 different internal clocks or an external clock can be selected as the transmit clock. The internal clocks include the six prescaler outputs divided by two and by four, and the system clock.
- During idle states, the serial output pin can be controlled to be high or low output
- Transmit clock errors can be detected
- An interrupt request can be generated after transfer has completed when an error occurs

Table 10 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

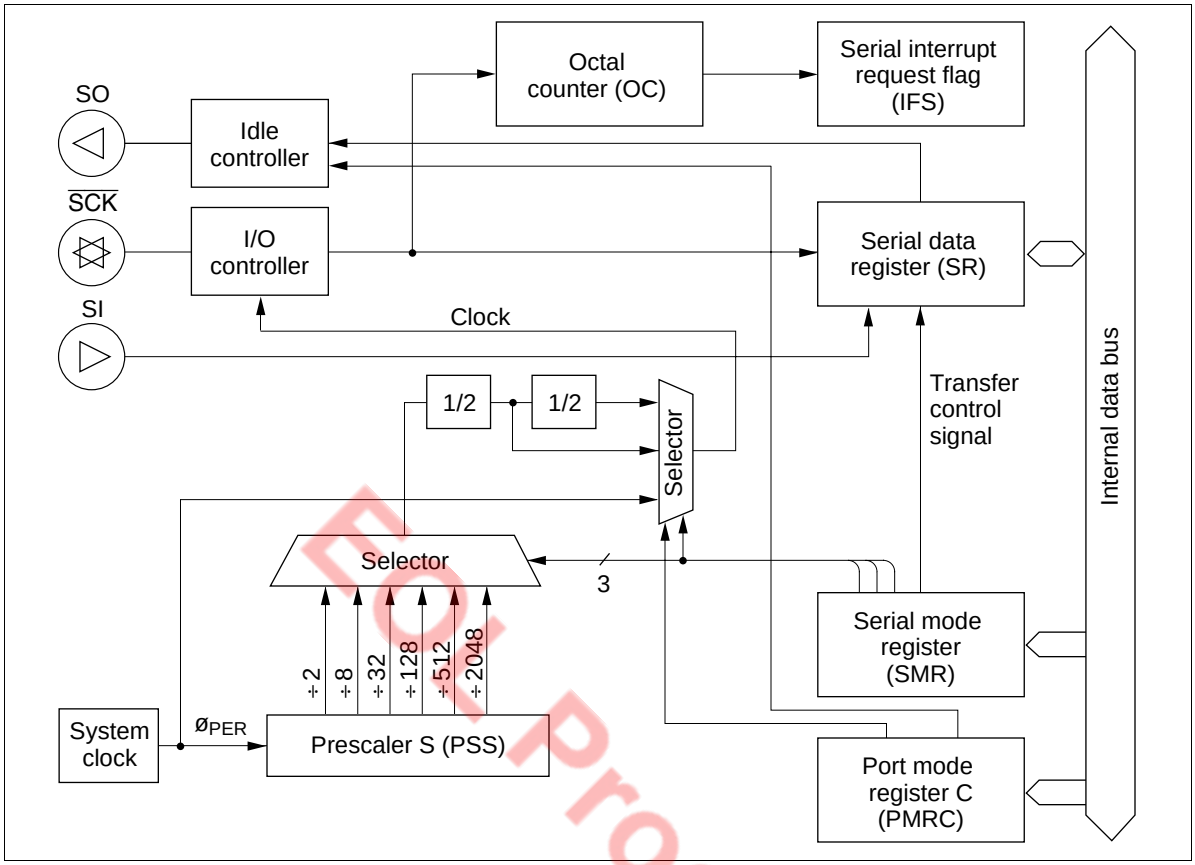


Figure 33 Serial Interface Block Diagram

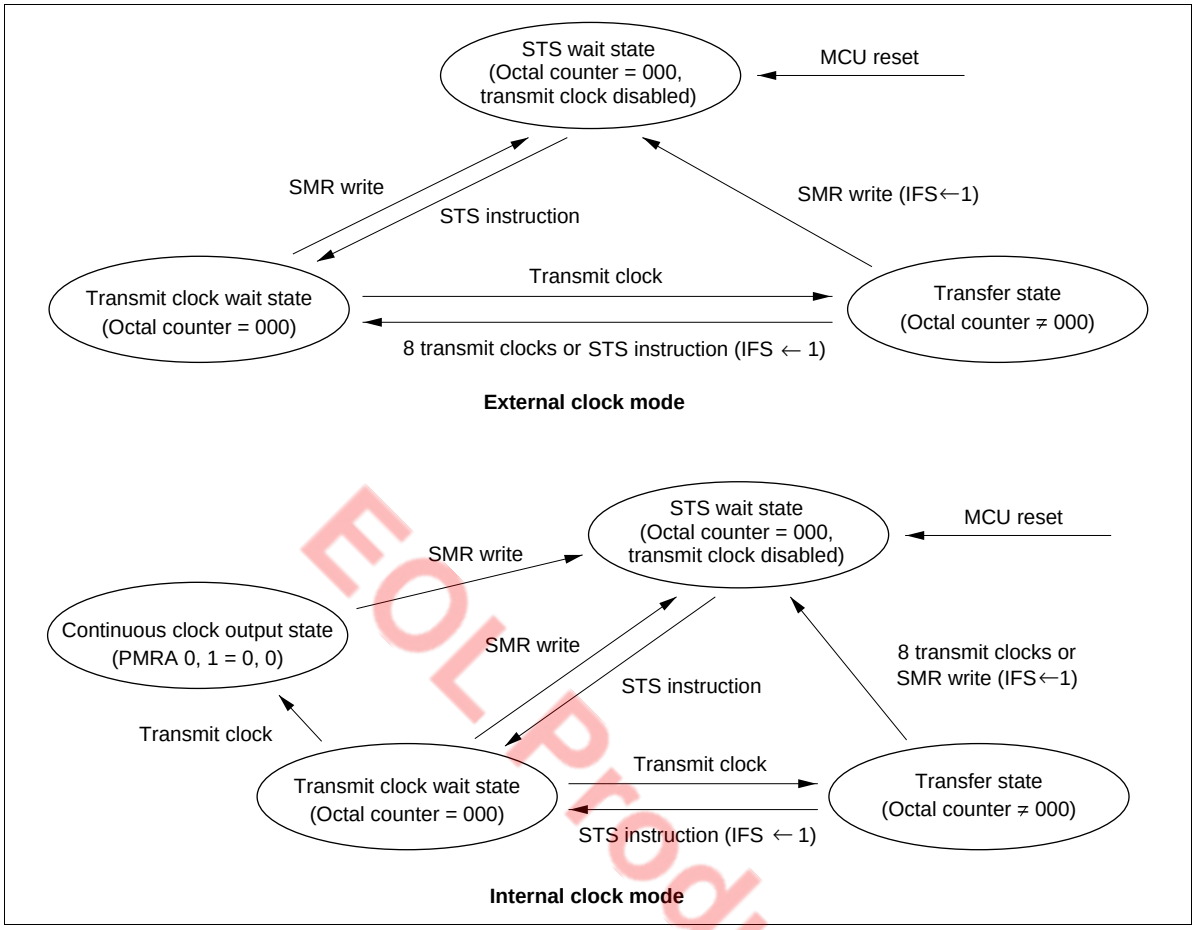


Figure 34 Serial Interface State Transitions

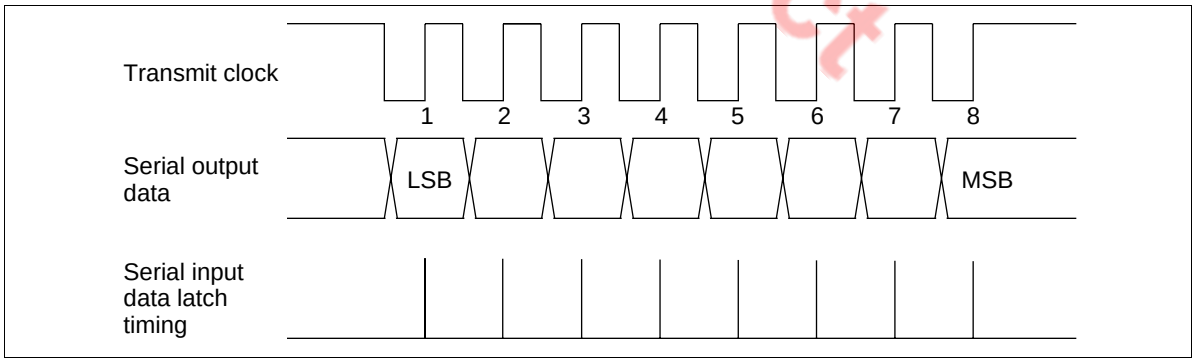


Figure 35 Serial Interface Timing

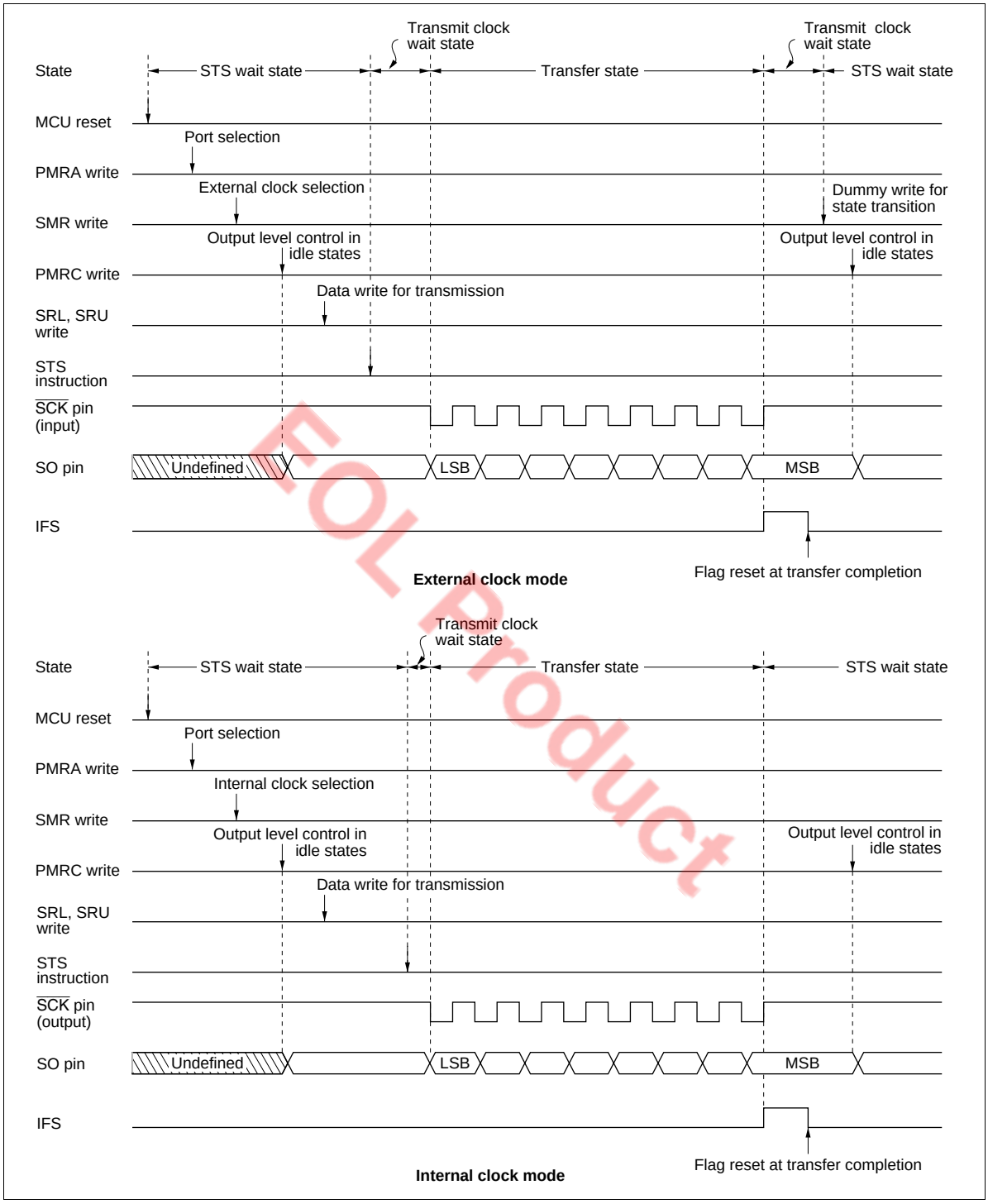


Figure 36 Example of Serial Interface Operation Sequence

Transmit clock erors are detected as illustrated in figure 37.

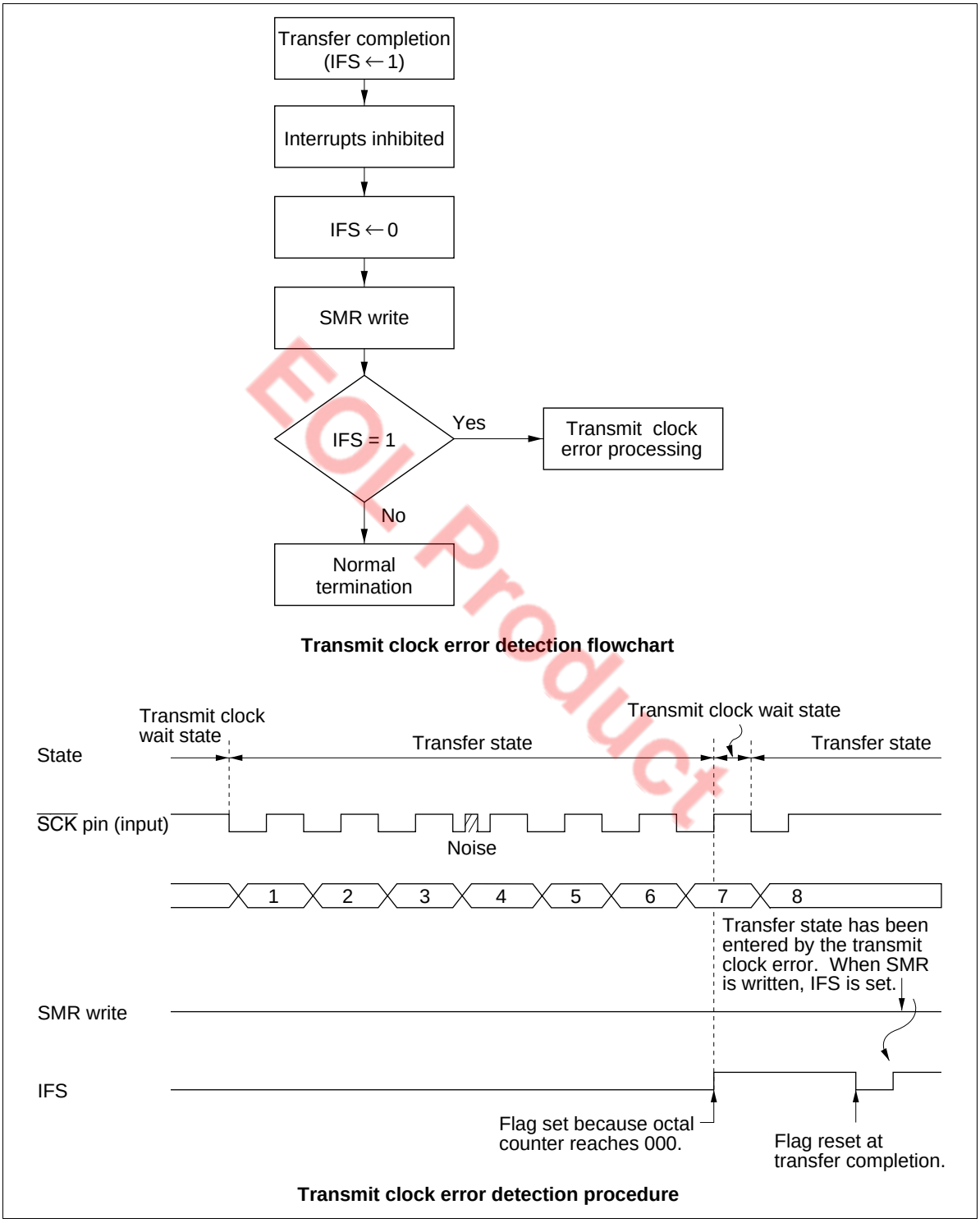


Figure 37 Transmit Clock Error Detection

Table 11 Transmit Clock Selection

PMRC	SMR				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**System Clock Divisor**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	Refer to table 11
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 38 Serial Mode Register (SMR)

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	Undefined	0
Read/Write	W	W	W	W
Bit name	PMRC3	PMRC2	PMRC1	PMRC0

Alarm output function.
Refer to table 9.

PMRC0	Serial Clock Division Ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

PMRC1	Output Level Control in Idle States
0	Low level
1	High level

Figure 39 Port Mode Register C (PMRC)

A/D Converter

The MCU also contains a built-in A/D converter that uses a sequential comparison method with a resistance ladder. It can perform digital conversion of eight analog inputs with 8-bit resolution. The following describes the A/D converter.

- A/D mode register 1 (AMR1: $019) is used to select digital or analog ports
- A/D mode register 2 (AMR2: $01A) is used to set the A/D conversion speed and to select digital or analog ports
- The A/D channel register (ACR: $016) is used to select an analog input channel
- A/D conversion is started by setting the A/D start flag (ADSF: $020, 2) to 1. After the conversion is completed, converted data is stored in the A/D data register, and at the same time, the A/D start flag is cleared to 0
- By setting the I_{AD} off flag (IAOF: $021, 2) to 1, the current flowing through the resistance ladder can be cut off even while operating in standby or active mode

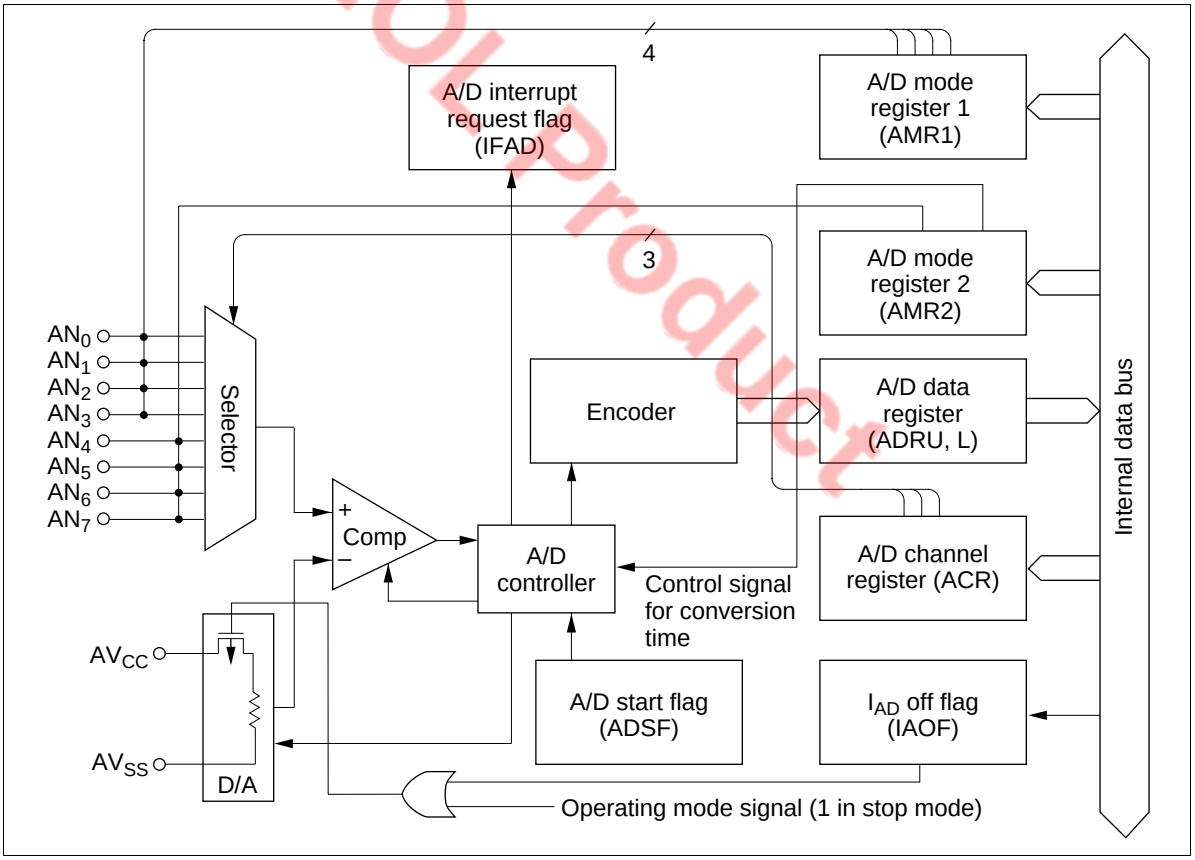


Figure 40 A/D Converter Block Diagram

Notes on Usage

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF)
- Do not write to the A/D start flag during A/D conversion
- Data in the A/D data register during A/D conversion is undefined
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop mode. In addition, to save power while in stop mode, all current flowing through the converter's resistance ladder is cut off.
- If the power supply for the A/D converter is to be different from V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to V_{CC}. When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by bit 1 of the A/D mode register as an analog pin will remain pulled up.

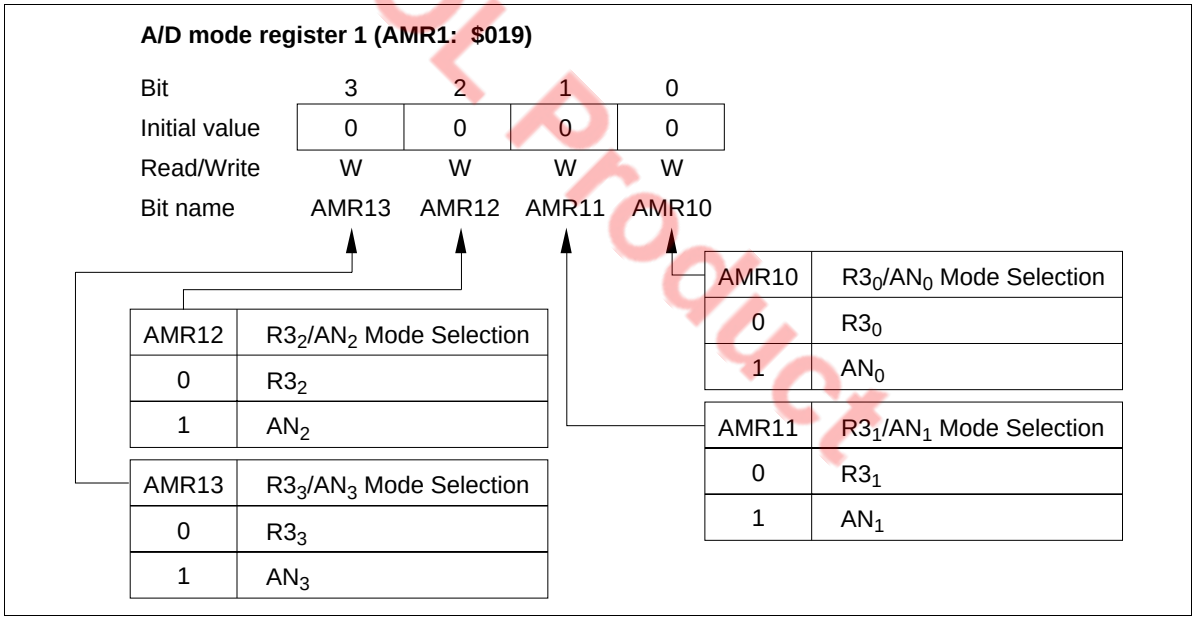


Figure 41 A/D Mode Register 1 (AMR1)

A/D mode register 2 (AMR2: $01A)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	AMR21	AMR20

AMR20	Conversion Time
0	$34t_{cyc}$
1	$67t_{cyc}$

AMR21	R4/AN_4–AN_7 Pin Selection
0	R4
1	AN_4–AN_7

Figure 42 A/D Mode Register (AMR2)

A/D channel register (ACR: $016)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	ACR2	ACR1	ACR0

ACR2	ACR1	ACR0	Analog Input Selection
0	0	0	AN_0
		1	AN_1
	1	0	AN_2
		1	AN_3
1	0	0	AN_4
		1	AN_5
	1	0	AN_6
		1	AN_7

Figure 43 A/D Channel Register (ACR)

A/D start flag (ADSF: $020, bit 2)

Bit	3	2	1	0
Initial value	—	0	0	—
Read/Write	—	R/W	W	—
Bit name	Not used	ADSF	WDON	Not used

A/D Start Flag (ADSF)	
0	A/D conversion completed
1	A/D conversion started

WDON
Refer to the description of timers

Figure 44 A/D Start Flag (ADSF)

I_{AD} off flag (IAOF: $021, bit 2)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	RAME	IAOF	ICEF	ICSF

I_{AD} Off Flag (IAOF)	
0	I_{AD} current flows
1	I_{AD} current is cut off

ICSF
Refer to the description of timers

ICEF
Refer to the description of timers

RAME
Refer to the description of operating modes

Figure 45 I_{AD} Off Flag (IAOF)

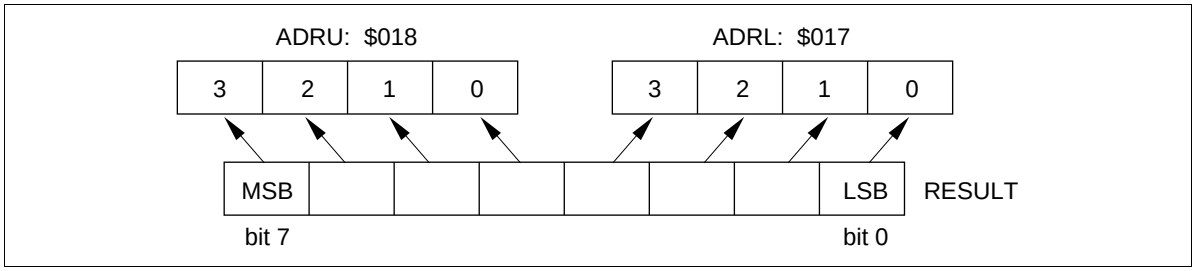


Figure 46 A/D Data Registers

A/D data register (lower digit) (ADRL: $017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	R	R	R
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

Figure 47 A/D Data Register Lower Digit (ADRL)

A/D data register (upper digit) (ADRU: $018)

Bit	3	2	1	0
Initial value	1	0	0	0
Read/Write	R	R	R	R
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

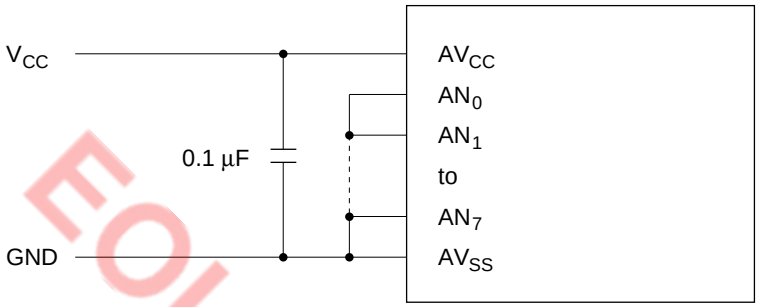
Figure 48 A/D Data Register Upper Digit (ADRU)

Notes on Mounting

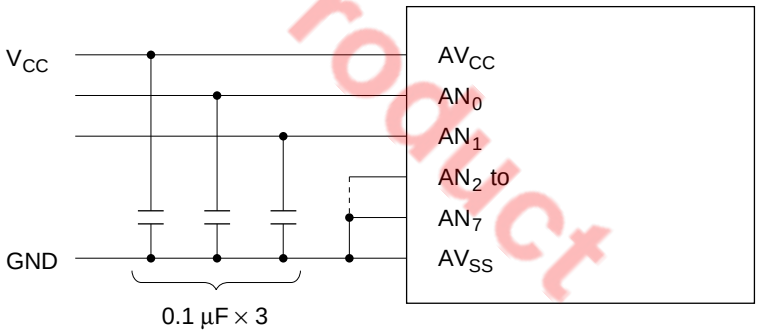
Assemble all parts including the HD404318 Series on a board, noting the points described below.

1. Connect layered ceramic type capacitors (about 0.1 µF) between AV_{CC} and AV_{SS}, between V_{CC} and GND, and between used analog pins and AV_{SS}.
2. Connect unused analog pins to AV_{SS}.

1. When not using an A/D converter.



2. When using pins AN_0 and AN_1 but not using AN_2 to AN_7.



3. When using all analog pins.

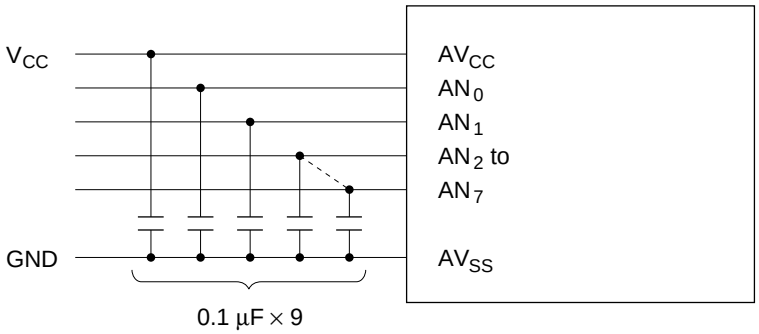


Figure 49 Example of Connections (1)

Between the V_{CC} and GND lines, connect capacitors designed for use in ordinary power supply circuits. An example connection is described in figure 50.

No resistors can be inserted in series in the power supply circuit, so the capacitors should be connected in parallel. The capacitors are a large capacitance C_1 and a small capacitance C_2.

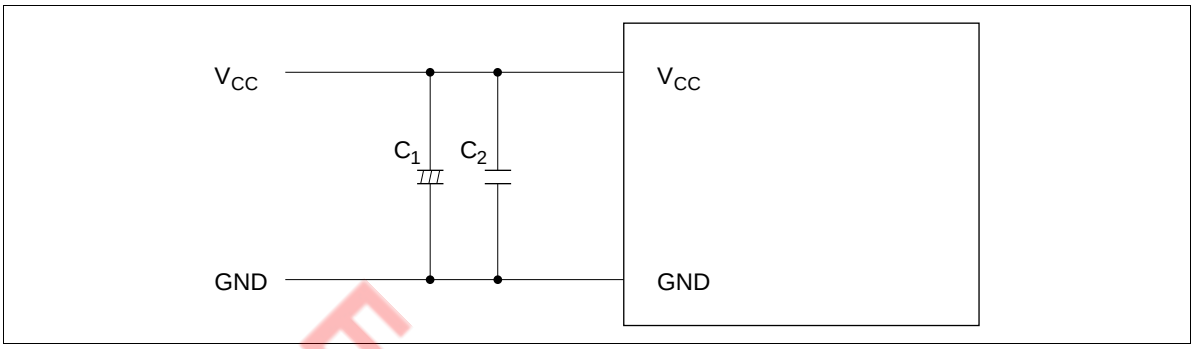


Figure 50 Example of Connections (2)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		V_{CC} – 45 to V_{CC} + 0.3	V	3
Total permissible input current	$\sum I_O$	70	mA	4
Total permissible output current	$-\sum I_O$	150	mA	5
Maximum input current	I_O	4	mA	6, 7
		20	mA	6, 8
Maximum output current	$-I_O$	4	mA	9, 10
		30	mA	10, 11
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST (V_{PP}) of HD4074318.
2. Applies to all standard voltage pins.
3. Applies to high-voltage pins.
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to ports R3 and R4.
8. Applies to port R0.
9. Applies to ports R0, R3, and R4.
10. The maximum output current is the maximum current flowing from V_{CC} to each I/O pin.
11. Applies to ports D_0–D_8, R1, R2, and R8.

Electrical Characteristics

DC Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, SI, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	0.8V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, SI	–0.3	—	0.2V_{CC}	V		
		$\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	V_{CC} – 40	—	0.2V_{CC}	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, SI, SO, TOC, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		$\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	—	—	20	µA	V_{in} = V_{CC} – 40 to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5
			—	—	8.0	mA		2, 6
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	V_{CC} = 5 V	4, 5
			—	—	20	µA		4, 6
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excludes current flowing through pull-up MOS and output buffers.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.

Test conditions: MCU: Reset
Pins: $\overline{RESET}$, TEST at GND
R0, R3, R4 at V_{CC}
D_0–D_8, R1, R2, R8, RA_1 at V_{disp}

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions: MCU: I/O reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   R0, R3, R4 at V_{CC}
   D_0–D_8, R1, R2, R8, RA_1 at V_{disp}
4. This is the source current when no I/O current is flowing.
   Test conditions: Pins: R0, R3, R4 at V_{CC}
   D_0–D_8, R1, R2, R8, RA_1 at GND
5. Applies to the HD404314, HD404316 and HD404318.
6. Applies to the HD4074318.

I/O Characteristics for Standard Pins (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R0, R3, R4	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	R0, R3, R4	–0.3	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	R0, R3, R4	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	R3, R4	—	—	0.4	V	I_{OL} = 1.6 mA	
		R0	—	—	2.0	V	I_{OL} = 10 mA	
Input leakage current	$\|I_{IL}\|$	R0, R3, R4	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS	$-I_{PU}$	R0, R3, R4	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	2
			30	80	180	µA		3

Notes: 1. Output buffer current is excluded.
2. Applies to the HD404314, HD404316, and HD404318.
3. Applies to the HD4074318.

I/O Characteristics for High-Voltage Pins (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_8, R1, R2, R8, RA_1	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_8, R1, R2, R8, RA_1	V_{CC} – 40	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_0–D_8, R1, R2, R8, BUZZ	V_{CC} – 3.0	—	—	V	–I_{OH} = 15 mA	
			V_{CC} – 2.0	—	—	V	–I_{OH} = 10 mA	
			V_{CC} – 1.0	—	—	V	–I_{OH} = 4 mA	
Output low voltage	V_{OL}	D_0–D_8, R1, R2, R8, BUZZ	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
			—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
I/O leakage current	$\|I_{IL}\|$	D_0–D_8, R1, R2, R8, RA_1, BUZZ	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_0–D_8, R1, R2, R8, BUZZ	200	600	1000	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applies to pins with pull-down MOS as selected by the mask option .
2. Applies to pins without pull-down MOS as selected by the mask option.
3. Excludes output buffer current.

A/D Converter Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0–AN_7	AV_{SS}	—	AV_{CC}	V		
Current flowing between AV_{CC} and AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0–AN_7	—	—	30	pF		
Resolution			8	8	8	Bit		
Number of input channels			0	—	8	Channel		
Absolute accuracy			—	—	±2.0	LSB		
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0–AN_7	1	—	—	MΩ		

Note: 1. Connect this to V_{CC} if the A/D converter is not used.

AC Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	System clock divided by 4	
Instruction cycle time	t_{cyc}		0.89	1	10	µs		
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		1
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		1
External clock high width	t_{CPH}	OSC_1	92	—	—	ns		2
External clock low width	t_{CPL}	OSC_1	92	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT}_0$, $\overline{INT}_1$, EVNB high widths	t_{IH}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT}_0$, $\overline{INT}_1$, EVNB low widths	t_{IL}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}		3
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		5
Input capacitance	C_{in}	All input pins except TEST	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	30	pF		6
			—	—	180	pF		7

Notes: 1. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:
a. After V_{CC} reaches 4.0 V at power-on.
b. After $\overline{RESET}$ input goes low when stop mode is cancelled.
c. After $\overline{STOPC}$ input goes low when stop mode is cancelled.
To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{RESET}$ or $\overline{STOPC}$ must be input for at least a duration of t_{RC}.
When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.
2. Refer to figure 51.
3. Refer to figure 52.
4. Refer to figure 53.
5. Refer to figure 54.
6. Applies to the HD404314, HD404316, and HD404318.
7. Applies to the HD4074318.

Serial Interface Timing Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	Load shown in figure 56	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 56	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 56	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 56	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 56	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 56	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 56	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. Refer to figure 55.

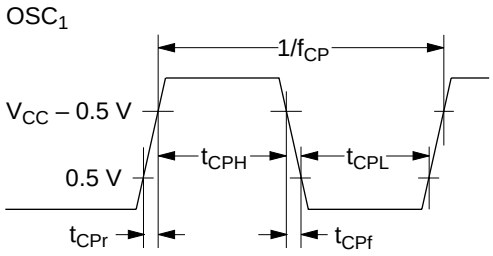


Figure 51 External Clock Timing

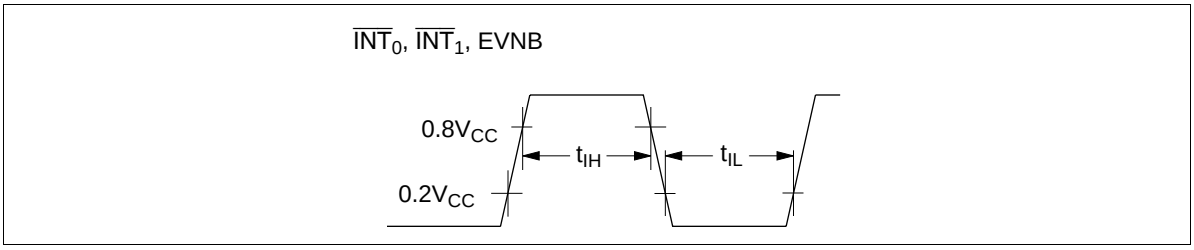


Figure 52 Interrupt Timing

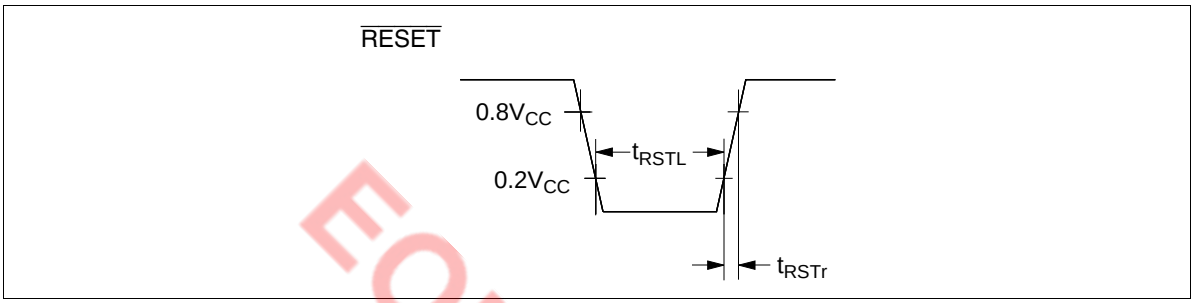


Figure 53 $\overline{\text{RESET}}$ Timing

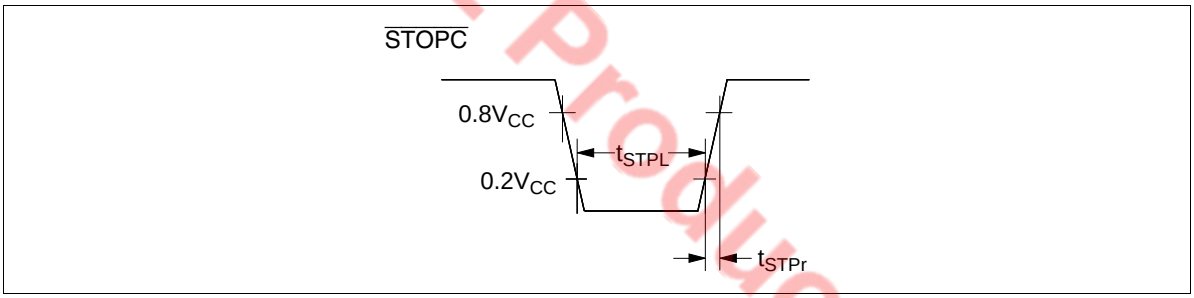
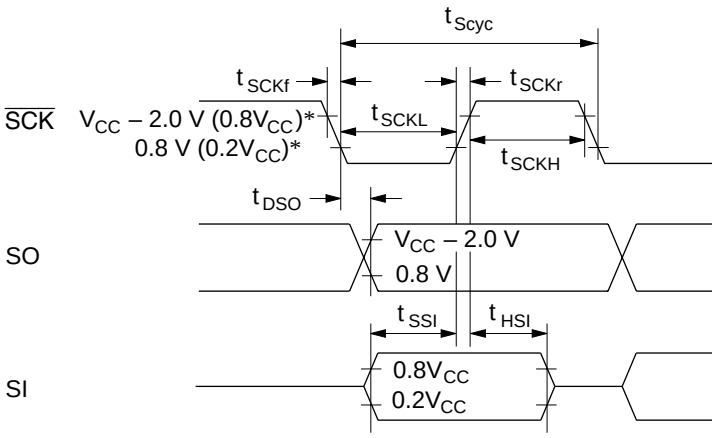


Figure 54 $\overline{\text{STOPC}}$ Timing



Note: *V_{CC}-2.0V and 0.8V are the threshold voltages for transmit clock output.
$0.8V_{CC}$ and $0.2V_{CC}$ are the threshold voltages for transmit clock input.

Figure 55 Serial Interface Timing

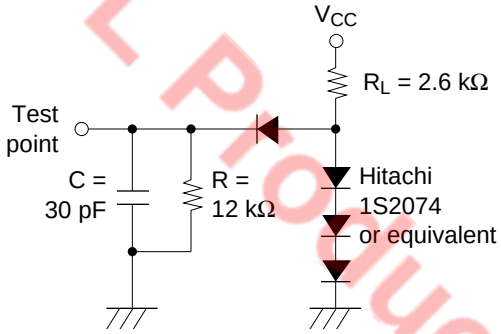


Figure 56 Timing Load Circuit

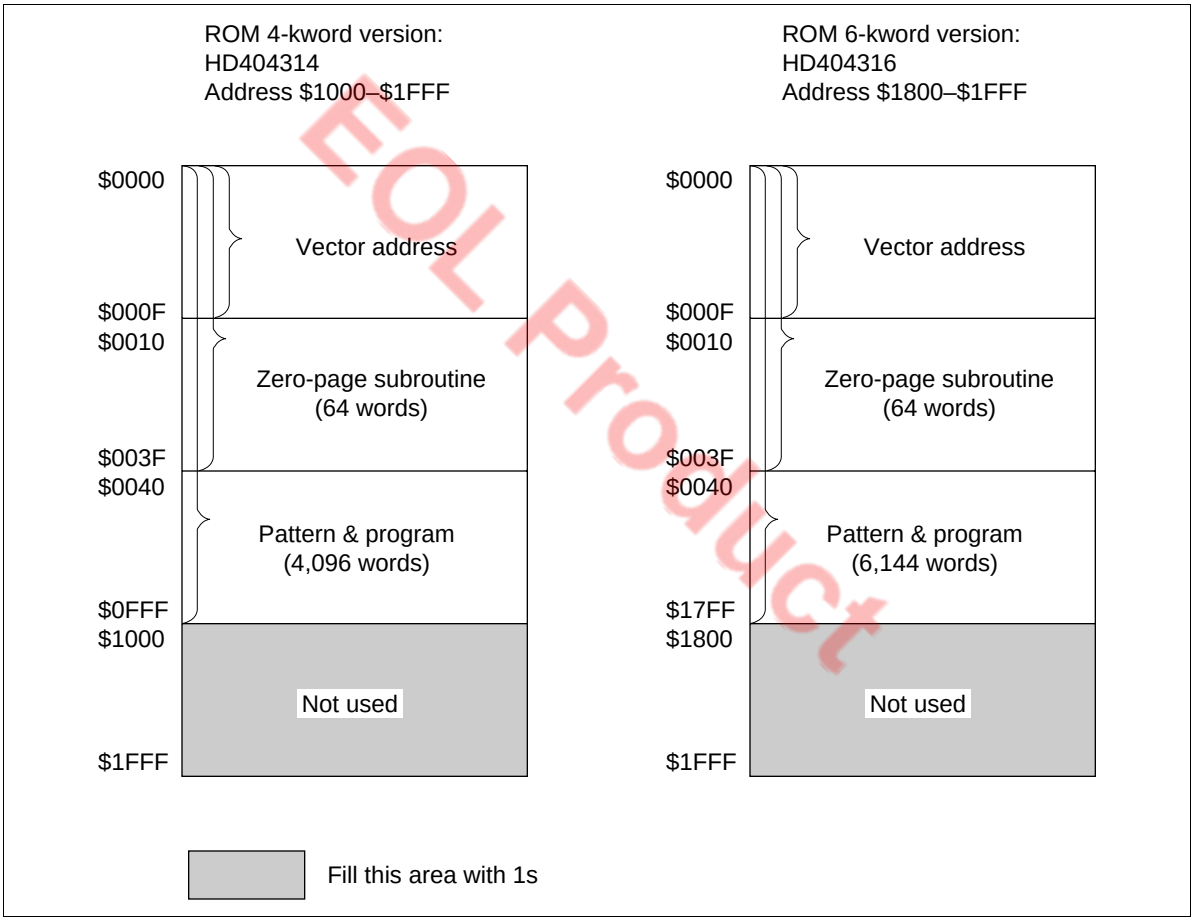
Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404314 and HD404316 as an 8-kword version

(HD404318). An 8-kword data size is required to change ROM data to mask manufacturing data since the program used is for an 8-kword version.

This limitation applies when using an EPROM or a data base.



HD404314/HD404316/HD404318 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM Size

☐ HD404314	4-kword
☐ HD404316	6-kword
☐ HD404318	8-kword

2. I/O Options

D: Without pull-down resistance

Pin name	I/O	I/O option D	I/O option E
D0/$\overline{INT0}$	I/O		
D1/$\overline{INT1}$	I/O		
D2/EVNB	I/O		
D3/BUZZ	I/O		
D4/$\overline{STOPC}$	I/O		
D5	I/O		
D6	I/O		
D7	I/O		
D8	I/O		

E: With pull-down resistance

Pin name		I/O	I/O option D	I/O option E
R1	R10	I/O		
	R11	I/O		
	R12	I/O		
	R13	I/O		
R2	R20	I/O		
	R21	I/O		
	R22	I/O		
	R23	I/O		
R8	R80	I/O		
	R81	I/O		
	R82	I/O		
	R83	I/O		
RA	RA1	I	Selected in option (3)	

3. RA1/Vdisp

☐ RA1 without pull-down resistance
☐ Vdisp

Note: If even only one pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

4. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System Oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

6. Stop mode

☐ Used
☐ Not used

7. Package

☐ DP-42S
☐ FP-44A

Cautions

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